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The nonlinear effect in the performance of 4:2 Compressor

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Abstract

In this article, we have designed a novel 4:2 QCA Compressor with a nonlinear effect. This can be considered as a new vision to design approximate Majority circuits with more than five-input. The main advantages of these ideas are the reduced number of QCA cells as well as power dissipation, increased speed, and improved cell area In addition, a novel hierarchy is introduced to optimize digital systems. The 4:2 Compressor circuit is selected as a benchmark. This circuit is simulated with some technologies such as CMOS, CNT, and QCA in different architectures. All results from power respective were compared. We have used QCADesigner and QCAPro for QCA Circuits, Hspice with 20nm-nfet PTM-MG model for CMOS circuits and Stanford CNFET 20nm model for CNT circuits as simulation tools to evaluate circuits.

Keywords: QCA, CNT, CMOS, The nonlinear effect, 4:2 Compressor, n -input Majority circuit, Approximate Circuit, Power Consumption.
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1. Introduction

In the last decades, the digital circuits industry has indicated the rapid growth of integrated circuits. Arithmetic operations have many applications in microprocessors and digital systems. The multiplication is a basic arithmetic operation in applications like digital signal processing [1, 23, 25]. This operator affects principal units like the arithmetic logic unit (ALU) and floating point unit.

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These operators execute operations such as convolution and filtering [10, 25]. In multipliers, the generation of partial products (GPP), reduction of partial products (RPP), and computing the final result are the main actions. The Booth algorithm is typically used in GPP phase [10, 27]. In RPP phase, CSA (Carry Save Adder) is used. This step is done with algorithms such as Wallace tree for fast multipliers or Dadda tree for designs with less hardware [12, 21].To compute the final result, Carry Propagate Adder (CPA) or a Carry Look-ahead Adder is used [10, 11]; which is the most common type to improve Carry propagation delay [15]. Reducing the partial products (the second phase) has a significant role in the overall delay, area, and power dissipation [8,13]. In most of these implementations, Compressors are used to reduce the critical path of circuits [15, 16, 19]. The use of digital Compressors such as 4:2 Compressors was introduced by Weinberger [16].

There are some techniques to reduce power consumption in digital systems. These techniques are divided into two groups; external and internal. External techniques deal with input data characteristics, while internal techniques correlate with the architecture, logic and circuit designs. Having a comprehensive viewpoint on internal techniques leads to more advantages over external ones. The first step to optimize digital systems is to improve the performance of arithmetic circuits. The second and third steps belongs to the algorithm and its related architecture, respectively. In the fourth step, modules should be optimized and in the last stage, elements could be improved (see Figure 1). This process is illustrated as follow.

For example we can use multiplication instead of the shift left operation. If the operation is accomplished by multiplying, multiplication operation would be done through different algorithms such as Booth, etc. Then in the next step, it must be indicated that what kind of architectures can be applied in designing Adders, Counters or Compressors. The fourth stage shows which module can be used as the basic Adder cell. In other words, which XOR modules is more suitable to implement the circuit. Finally, embedded elements in the modules will be selected. Nowadays, we have several options for elements (devices). According to [7], the beyond CMOS circuits are divided into two groups: transistor circuits (TCs) and Majority gate circuits (MGs). The TC such as MOSFETs and Carbon Nanotube (CNT), and the MG such as quantum dot cellular automata (QCAs). However, the type of devices plays an important role in performance; whilst the size of transistors or other characteristics could have a serious impact on the optimum circuit design. Moreover, we have limitations on the size of the transistor. In other words, the distance between source and drain cannot be less than one Ion.

In this article, evaluating the third and fifth steps of the proposed hierarchy has been done. Therefore, the different architectures of 4:2 Compressor (as a benchmark) were selected under several devices (technologies). In addition, the novel implementation of the 4:2 QCA Compressor circuit was proposed.

The rest of this paper is organized as follows: section (2), covers a brief overview of 4:2 Compressors, QCA and CNT. Section (3) discusses the various architectures of 4:2 Compressors. Then, a novel 4:2 QCA Compressor implementation is proposed. Subsequently, the different 4:2 Compressors (with various architecture and elements) are evaluated in section (5). Finally, section (6) presents the conclusion.

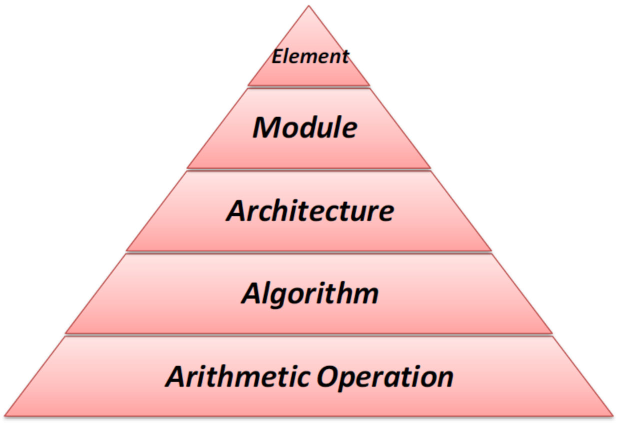


Figure 1: The proposed hierarchy to optimize digital systems.

2. Background

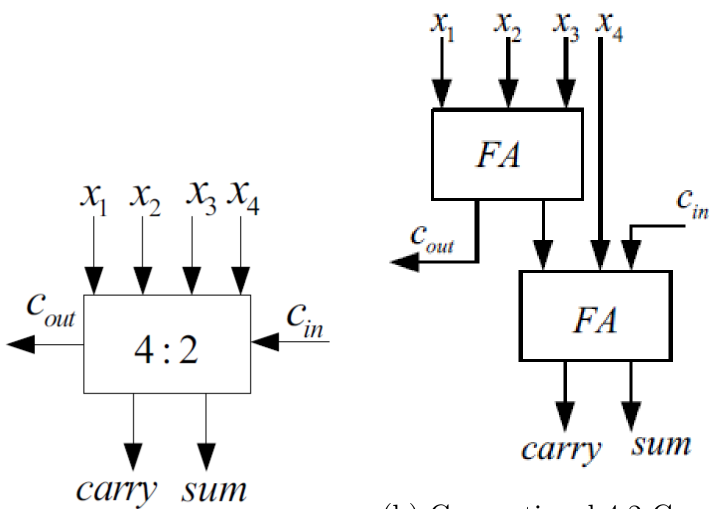
In this section, the structure of 4:2 Compressor, CNT and QCA is discussed which includes the basic target of our study.

2.1. The 4:2 Compressors

A 4:2 Compressor has four inputs (X_1, X_2, X_3, X_4) as well as two outputs (Sum, Carry), along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Figure 2a. The Cin signal is the output from the previous lower significant stage and the Cout is the input signal (as Cin) to the next significant stage. Various structures of 4:2 Compressors are available; however, they are demonstrated by the principal Equation given as follows [10]:

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2(Carry + C_{out}). \tag{2.1}$$

The first presentation of the 4:2 Compressor is designed by two cascaded Full Adders (FA) as illustrated in Figure 2b [11].



(a) A Compressor 4:2

(b) Conventional 4:2 Compressor with 4Δ

Figure 2: (a) A Compressor 4:2, (b) Conventional 4:2 Compressor with 4Δ

2.2. The Carbon Nano Tube (CNT) technology:

CNT is a cylindrical sheet of graphite formed geometrically in two forms: Single-Walled Carbon NanoTubes (SWCNTs) that is made from a cylinder; and Multi-Walled Carbon NanoTubes (MWCNTs) which is made from more than one cylinder. These cylinders are named tubes.
The band gap in CNTFETs is described in Equation (2.2). In this equation vth is threshold voltage and d is diagonal. Moreover, the width of the gate terminal in CNFET is achieved from Equation (2.3) in which N is the number of Nanotubes in the channel, Pitch shows the distance between two neighborhood Nanotubes with the same channel, and DCNT is the diameter of Nano tubes [3, 14].

$$V_{th} = \frac{0.42}{d_{nm}} \tag{2.2}$$

$$W_{gate} = (N-1)Pitch + DCNT \tag{2.3}$$

2.3. The Quantum dot Cellular Automata (QCA) technology:

The basic element in quantum dot cellular automata is a cell with four dots and two mobile electrons (see Figure 3a). These electrons are in the opposite corners which could have two possible polarizations ($P = +1, P = -1$) In QCA, the position of electrons made logical states and these are independent of the voltage level. The basic gates in QCA circuits are inverter and Majority gates. In Figure 3b and Figure 4, three-input Majority function and some common inverters have been illustrated, respectively [8, 9]. The logical function of a Majority gate is in (2.4):

$$Maj(A,B,C) = AB + BC + AC \tag{2.4}$$

Setting the polarization of inputs gives two-input AND gate ($-1(logic\ 0)$) and two-input OR gate ($+1(logic\ 1)$). These Equations have been described in (2.5),(2.6) [4, 18, 22, 24].

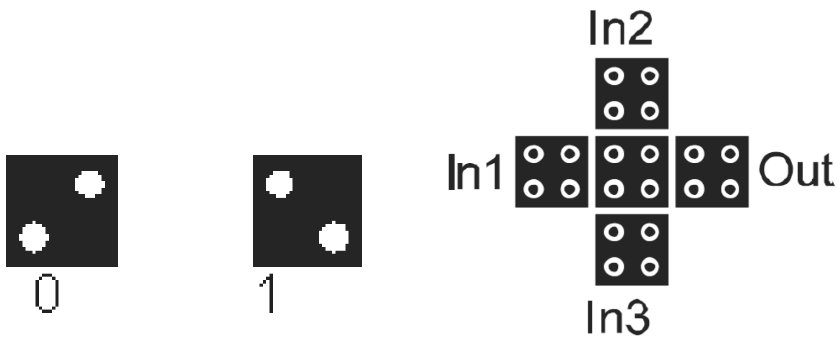
$$Maj(A,B,0) = AB + (A.B) + (B.0) = AB \tag{2.5}$$

$$Maj(A,B,1) = AB + (A.1) + B.1) = A + B \tag{2.6}$$

The energy of two cells i and j are shown in Equation (2.7). This equation is the outcome of calculating all charges that achieve electrostatic interactions. In fact, the electrostatic interactions generate as consequence of interactions between neighbor cells.

$$F_{i,j} = K\frac{q_i q_j}{r^2} \tag{2.7}$$

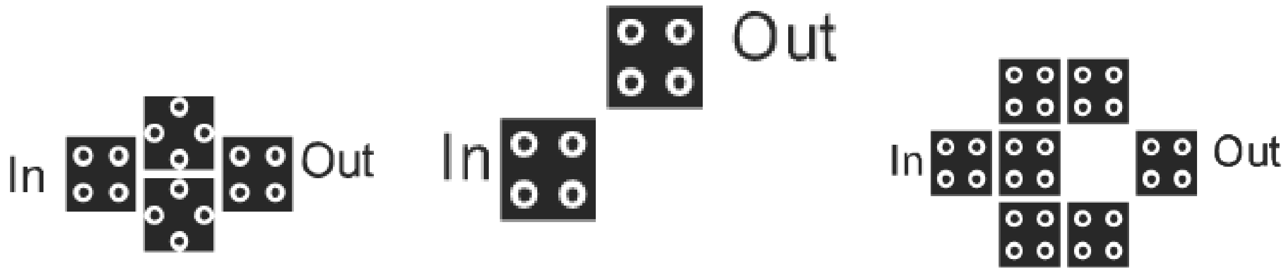
In (2.7), K is fixed colon, q_{i-j} is electron charge and r describes the distance between i, j cells.



(a) The basic logic cells in QCA with two possible polarization

(b) Three-input Majority function gate

Figure 3: The basic logic cells in QCA with two possible polarization



(a) Common Inverters in QCA (b) Reference[8] (c) Reference[9]

Figure 4: Common Inverters in QCA

3. The Architecture of 4:2Compressor

The First architecture is the decomposed logic of 4:2 Compressor shown in Figure 5. This design has a critical path delay of 3Δ (three-delay steps), which is 1Δ delay shorter than the conventional implementation (each FA has a critical path delay of $2Xor_2$ (see Figure 2b)) [26]. The equations of the Compressor, based on mentioned architecture, are described as following:

$$if : h = X_1 \oplus X_2 \oplus X_3 \oplus X_4$$

$$C_{out} = X_1\bar{X}_2 + X_1X_3 + \bar{X}_2X_3 \tag{3.1}$$

$$Carry = hX_4 + \bar{h}C_{in} \tag{3.2}$$

$$sum = h \oplus C_{in} \tag{3.3}$$

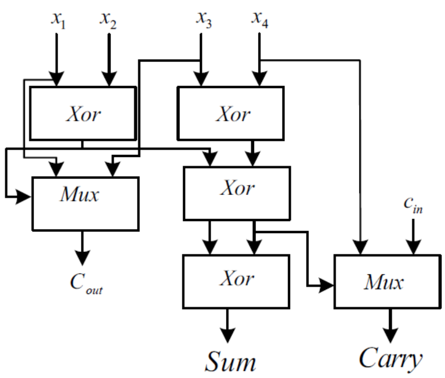


Figure 5: The architecture decomposition of 4:2 Compressor (design I).

The second design (design II) is shown in Figure 6. To reduce the delay propagation, the Cout signal has been produced without waiting for intermediate connections. The three-input Majority function is utilized for this target. In the next step, a reduction of the static hazard, glitch, and simplification are needed. This leads to lower power consumption; therefore, the pseudo-absorption law could be utilized. In Equations (3.4,3.5,3.6,3.7) this simplification has been shown [17].

$$\begin{aligned}
&C_{out} = Majority(X_1, X_2, X_3) && (3.4)\\
&if: h = X_1 \oplus X_2 \oplus X_3 &&\\
&Carry = (X_4 + C_{in})\bar{h} + X_4 C_{in} h && (3.5)\\
&\qquad\quad = X_4(C_{in}h + \bar{h}) + C_{in}\bar{h} &&\\
&\qquad\quad = X_4(C_{in} + \bar{h}) + C_{in}\bar{h} \qquad pseudo-absorptionlaw &&\\
&\qquad\quad = X_4 C_{in} + X_4\bar{h} + C_{in}\bar{h} &&\\
&Carry = Majority(X_4, C_{in}, \bar{h}) && (3.6)\\
&sum = X_4 \oplus C_{in} \oplus h && (3.7)
\end{aligned}$$

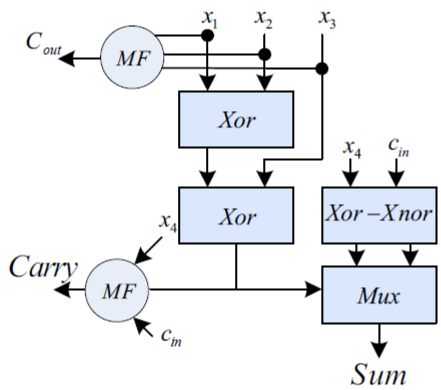


Figure 6: The structure of second architecture (design II).

Last design is only based on Majority function (design III). The three, seven, and nine-input Majority gates are needed to generate Cout, Carry and Sum signals, respectively. The mentioned design has less hardware and power consumption compared to other designs; however, it suffers from the more noise if suitable devices are not used in its design. Figure 7 and Equations (3.8,3.9,3.10,3.11) show the logic of this architecture [2].

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2(Carry + C_{out}) \tag{3.8}$$

$$C_{out} = Majority(X_1, X_2, X_3) \tag{3.9}$$

$$Carry = Majority(X_1, X_2, X_3, X_4, C_{in}, \bar{C}_{out}, \bar{C}_{out}) \tag{3.10}$$

$$Sum = Majority(X_1, X_2, X_3, X_4, C_{in}, \bar{C}_{out}, \bar{C}_{out}, \overline{Carry}, \overline{Carry}) \tag{3.11}$$

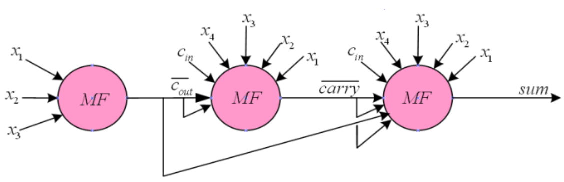


Figure 7: The Majority based Architecture (design III).

4. Our work:

Implementation Approach: When it is necessary to double the effect of signal, Equation can be used to obtain the required force [18]. It should be noted that the force and distance of the electrons have opposite relation. Reducing the distance between intercellular (less than 2nm) is contrary to the rules of technology; therefore, this idea can be implemented by reducing the force. In other words, when the double effect of the signal is needed, the distance is in its default state and when the effect of signal does not need to be increased the distance is increased, as a result, the force will be reduced. In order to prove the efficiency of this idea a 4:2 Compressor is designed.
Comparison Approach: As mentioned before, there are three disparate architectures to perform the 4:2 Compressors. We have called "design I, II, and III", respectively. In this research, each architecture is implemented with different devices (elements). These elements are (FET) CMOS, CNT, and QCA. CMOS is selected because it is consider as be the dominant technology; hence, each device should be compared with it. The CNT is a kind of FET; however, its characteristics and parameters are greatly improved [13]. In addition, since the changes in tube diagonal caused different threshold voltage, CNTs have more acceptable performance than MOSFETs in second and third design. Finally, QCA is a novel phenomenon that possesses excellent characteristics.
Physical Proof: Equations ((4.1),(4.2),(4.3),(4.4),(4.5),(4.6)) and Figure 8 show the Coulombic interactions between electrons. These calculations prove that the proposed structure acts as a seven-input Majority function (approximate behavior). Since the calculations are the same in each state, only one of the critical states is shown.
State four ("010110"), electron x_1, Figure 8a:

$$\begin{aligned}
&F_{1,x} = K\frac{q_i q_j}{r^2} \Rightarrow \frac{8.99\times10^{9}\times2.56\times10^{-38}}{((58)+(21)\times10^{-9})^2} = 0.006\times10^{-11}N \quad (a=48^\circ) \qquad (4.1)\\
&F_{2,x} \Rightarrow \frac{23.01\times10^{-29}}{((40)+(3)\times10^{-9})^2} = 0.014\times10^{-11}N \quad (a=4^\circ)\\
&F_{3,x} \Rightarrow \frac{23.01\times10^{-29}}{((20)\times10^{-9})^2} = 0.057\times10^{-11}N\\
&F_{4,x} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(2)\times10^{-9})^2} = 0.96\times10^{-11}N \quad (a=6^\circ)\\
&F_{5,x} \Rightarrow \frac{23.01\times10^{-29}}{(3\times10^{-9})^2} = 2.56\times10^{-11}\\
&F_{6,x} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(21)\times10^{-9})^2} = 0.03\times10^{-11}N \quad (a=40^\circ)\\
&F_{7,x} \Rightarrow \frac{23.01\times10^{-29}}{(21\times10^{-9})^2} = 0.052\times10^{-11}N\\
&F_{8,x} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(39)\times10^{-9})^2} = 0.012\times10^{-11}N \quad (a=65^\circ)\\
&F_{9,x} \Rightarrow \frac{23.01\times10^{-29}}{((40)+(21)\times10^{-9})^2} = 0.011\times10^{-11}N \quad (a=28^\circ)\\
&F_{10,x} \Rightarrow \frac{23.01\times10^{-29}}{((58)+(39)\times10^{-9})^2} = 0.005\times10^{-11}N \quad (a=34^\circ)
\end{aligned}$$

$$F_{11,x} \Rightarrow out\ of\ range$$

$$F_{12,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (61) \times 10^{-9})^2} = 0.006 \times 10^{-11}N \qquad (a = 16°)$$

$$F_{x_2} \Rightarrow \frac{23.01 \times 10^{-29}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11}N$$

$$F_{x_3} \Rightarrow \frac{23.01 \times 10^{-29}}{(40 \times 10^{-9})^2} = 0.014 \times 10^{-11}N$$

$$F_{tx_1} = (2.38i, -0.15j) \times 10^{-11}N$$

State four ("010110"), electron x_2:

$$F_{1,x} \Rightarrow \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((38) + (21) \times 10^{-9})^2} = 0.012 \times 10^{-11}N \qquad (a = 29°) \tag{4.2}$$

$$F_{2,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((20) + (3) \times 10^{-9})^2} = 0.056 \times 10^{-11}N \qquad (a = 9°)$$

$$F_{3,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((20) + (20) \times 10^{-9})^2} = 0.029 \times 10^{-11}N \qquad (a = 45°)$$

$$F_{4,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((2) + (2) \times 10^{-9})^2} = 2.87 \times 10^{-11}N \qquad (a = 45°)$$

$$F_{5,x} \Rightarrow \frac{23.01 \times 10^{-29}}{(23 \times 10^{-9})^2} = 0.04 \times 10^{-11}N$$

$$F_{6,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (41) \times 10^{-9})^2} = 0.011 \times 10^{-11}N \qquad (a = 23°)$$

$$F_{7,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((21) + (18) \times 10^{-9})^2} = 0.03 \times 10^{-11}N \qquad (a = 40°)$$

$$F_{8,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((2) + (39) \times 10^{-9})^2} = 0.015 \times 10^{-11}N \qquad (a = 3°)$$

$$F_{9,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((2) + (21) \times 10^{-9})^2} = 0.05 \times 10^{-11}N \qquad (a = 84.5°)$$

$$F_{10,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((20) + (39) \times 10^{-9})^2} = 0.012 \times 10^{-11}N \qquad (a = 63°)$$

$$F_{11,x} \Rightarrow \frac{23.01 \times 10^{-29}}{(59 \times 10^{-9})^2} = 0.006 \times 10^{-11}N$$

$$F_{12,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (23) \times 10^{-9})^2} = 0.027 \times 10^{-11}N \qquad (a = 38°)$$

$$F_{x_1} \Rightarrow \frac{23.01 \times 10^{-29}}{((20) + (3) \times 10^{-9})^2} = 0.056 \times 10^{-11}N \qquad (a = 9°)$$

$$F_{x_3} \Rightarrow \frac{23.01 \times 10^{-29}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11}N$$

$$F_{tx_2} = (1.26i, 1.94j) \times 10^{-11}N$$

State four (“010110”), electron x_3:

$$F_{1,x} \Rightarrow \frac{8.99 \times 10^{9} \times 2.56 \times 10^{-38}}{((18) + (21) \times 10^{-9})^2} = 0.030 \times 10^{-11} N \qquad (a = 49^\circ) \tag{4.3}$$

$$F_{2,x} \Rightarrow \frac{23.01 \times 10^{-29}}{(3 \times 10^{-9})^2} = 2.56 \times 10^{-11} N$$

$$F_{3,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((40) + (20) \times 10^{-9})^2} = 0.03 \times 10^{-11} N \qquad (a = 27^\circ)$$

$$F_{4,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((22) + (2) \times 10^{-9})^2} = 0.047 \times 10^{-11} N \qquad (a = 5^\circ)$$

$$F_{5,x} \Rightarrow \frac{23.01 \times 10^{-29}}{(43 \times 10^{-9})^2} = 0.012 \times 10^{-11} N$$

$$F_{6,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (61) \times 10^{-9})^2} = 0.006 \times 10^{-11} N \qquad (a = 16^\circ)$$

$$F_{7,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((40) + (21) \times 10^{-9})^2} = 0.011 \times 10^{-11} N \qquad (a = 28^\circ)$$

$$F_{8,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((22) + (39) \times 10^{-9})^2} = 0.011 \times 10^{-11} N \qquad (a = 60^\circ)$$

$$F_{9,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((21) \times 10^{-9})^2} = 0.052 \times 10^{-11} N \qquad (a = 84.5^\circ)$$

$$F_{10,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (39) \times 10^{-9})^2} = 0.012 \times 10^{-11} N \qquad (a = 65^\circ)$$

$$F_{11,x} \Rightarrow \frac{23.01 \times 10^{-29}}{(39 \times 10^{-9})^2} = 0.015 \times 10^{-11} N$$

$$F_{12,x} \Rightarrow \frac{23.01 \times 10^{-29}}{((18) + (21) \times 10^{-9})^2} = 0.03 \times 10^{-11} N \qquad (a = 40^\circ)$$

$$F_{x_1} \Rightarrow \frac{23.01 \times 10^{-29}}{(40 \times 10^{-9})^2} = 0.014 \times 10^{-11} N$$

$$F_{x_2} \Rightarrow \frac{23.01 \times 10^{-29}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11} N$$

$$F_{tx_3} = (0.1i, -2.49j) \times 10^{-11} N$$

$$F_{tx} = (3.75i, -4.58j) \times 10^{-11} N$$

State four ("010110"), electron y_1, Figure 8b:

$$F_{1,y} \Rightarrow \frac{8.99\times10^{9}\times2.56\times10^{-38}}{((39)+(40)\times10^{-9})^2}=0.007\times10^{-11}N \qquad (a=44^\circ) \tag{4.4}$$
$$F_{2,y} \Rightarrow \frac{23.01\times10^{-29}}{((22)+(21)\times10^{-9})^2}=0.024\times10^{-11}N \qquad (a=43^\circ)$$
$$F_{3,y} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(38)\times10^{-9})^2}=0.012\times10^{-11}N \qquad (a=25^\circ)$$
$$F_{4,y} \Rightarrow \frac{23.01\times10^{-29}}{((20)\times10^{-9})^2}=0.057\times10^{-11}N$$
$$F_{5,y} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(21)\times10^{-9})^2}=0.03\times10^{-11}N \qquad (a=40^\circ)$$
$$F_{6,y} \Rightarrow \frac{23.01\times10^{-29}}{(39\times10^{-9})^2}=0.015\times10^{-11}N$$
$$F_{7,y} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(3)\times10^{-9})^2}=0.069\times10^{-11}N \qquad (a=9^\circ)$$
$$F_{8,y} \Rightarrow \frac{23.01\times10^{-29}}{(21\times10^{-9})^2}=0.052\times10^{-11}N$$
$$F_{9,y} \Rightarrow \frac{23.01\times10^{-29}}{((3)+(22)\times10^{-9})^2}=0.047\times10^{-11}N \qquad (a=9^\circ)$$
$$F_{10,y} \Rightarrow \frac{23.01\times10^{-29}}{((40)+(21)\times10^{-9})^2}=0.011\times10^{-11}N \qquad (a=28^\circ)$$
$$F_{11,y} \Rightarrow \frac{23.01\times10^{-29}}{((61)+(18)\times10^{-9})^2}=0.0057\times10^{-11}N \qquad (a=16^\circ)$$
$$F_{12,y} \Rightarrow \frac{23.01\times10^{-29}}{(43\times10^{-9})^2}=0.012\times10^{-11}N$$
$$F_{y_2} \Rightarrow \frac{23.01\times10^{-29}}{(20\times10^{-9})^2}=0.057\times10^{-11}N$$
$$F_{y_3} \Rightarrow \frac{23.01\times10^{-29}}{(40\times10^{-9})^2}=0.014\times10^{-11}N$$
$$F_{ty_1}=(-0.006i,-0.003j)\times10^{-11}N$$

State four ("010110"), electron y_2:

$$F_{1,y} \Rightarrow \frac{8.99\times10^{9}\times2.56\times10^{-38}}{((20)+(39)\times10^{-9})^2} = 0.011\times10^{-11}N \qquad (a=63^\circ) \tag{4.5}$$

$$F_{2,y} \Rightarrow \frac{23.01\times10^{-29}}{((2)+(21)\times10^{-9})^2} = 0.052\times10^{-11}N \qquad (a=84.5^\circ)$$

$$F_{3,y} \Rightarrow \frac{23.01\times10^{-29}}{((38)+(38)\times10^{-9})^2} = 0.008\times10^{-11}N \qquad (a=45^\circ)$$

$$F_{4,y} \Rightarrow \frac{23.01\times10^{-29}}{((20)+(2)\times10^{-9})^2} = 0.057\times10^{-11}N \qquad (a=84^\circ)$$

$$F_{5,y} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(23)\times10^{-9})^2} = 0.016\times10^{-11}N \qquad (a=38^\circ)$$

$$F_{6,y} \Rightarrow \frac{23.01\times10^{-29}}{(59\times10^{-9})^2} = 0.007\times10^{-11}N$$

$$F_{7,y} \Rightarrow \frac{23.01\times10^{-29}}{((38)+(3)\times10^{-9})^2} = 0.016\times10^{-11}N \qquad (a=3^\circ)$$

$$F_{8,y} \Rightarrow \frac{23.01\times10^{-29}}{((21)+(20)\times10^{-9})^2} = 0.027\times10^{-11}N \qquad (a=46^\circ)$$

$$F_{9,y} \Rightarrow \frac{23.01\times10^{-29}}{((3)+(2)\times10^{-9})^2} = 1.8\times10^{-11}N \qquad (a=55^\circ)$$

$$F_{10,y} \Rightarrow \frac{23.01\times10^{-29}}{((2)+(21)\times10^{-9})^2} = 0.05\times10^{-11}N \qquad (a=84.5^\circ)$$

$$F_{11,y} \Rightarrow \frac{23.01\times10^{-29}}{((18)+(41)\times10^{-9})^2} = 0.011\times10^{-11}N \qquad (a=23^\circ)$$

$$F_{12,y} \Rightarrow \frac{23.01\times10^{-29}}{(23\times10^{-9})^2} = 0.043\times10^{-11}N$$

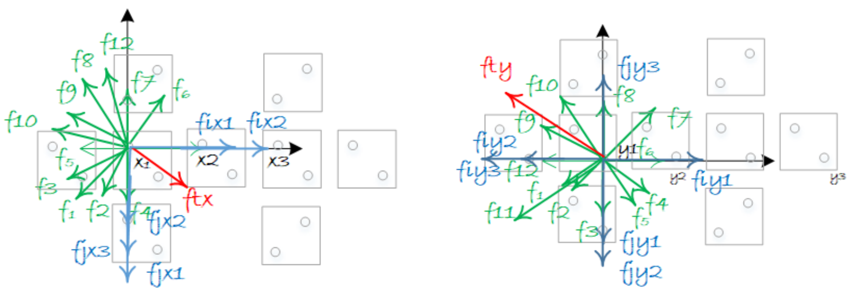
$$F_{y_1} \Rightarrow \frac{23.01\times10^{-29}}{(20\times10^{-9})^2} = 0.057\times10^{-11}N$$

$$F_{y_3} \Rightarrow \frac{23.01\times10^{-29}}{(20\times10^{-9})^2} = 0.057\times10^{-11}N$$

$$F_{ty_2} = (1.44i, -1.04j)\times10^{-11}N$$

State four ("010110"), electron y_3:

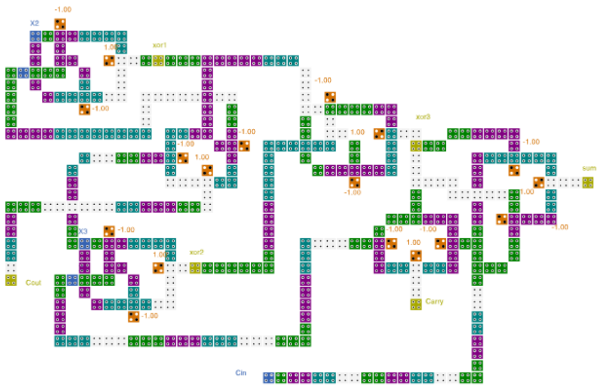
$$F_{1,y} \Rightarrow \frac{8.99 \times 10^{9} \times 2.56 \times 10^{-38}}{(39 \times 10^{-9})^2} = 0.016 \times 10^{-11} N \tag{4.6}$$
$$F_{2,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((18)+(21) \times 10^{-9})^2} = 0.03 \times 10^{-11} N \qquad (a = 49°)$$
$$F_{3,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((58)+(39) \times 10^{-9})^2} = 0.005 \times 10^{-11} N \qquad (a = 34°)$$
$$F_{4,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((21)+(40) \times 10^{-9})^2} = 0.011 \times 10^{-11} N \qquad (a = 28°)$$
$$F_{5,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((18)+(61) \times 10^{-9})^2} = 0.006 \times 10^{-11} N \qquad (a = 16°)$$
$$F_{6,y} \Rightarrow out\ of\ range$$
$$F_{7,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((58)+(3) \times 10^{-9})^2} = 0.0076 \times 10^{-11} N \qquad (a = 3°)$$
$$F_{8,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((21)+(22) \times 10^{-9})^2} = 0.02 \times 10^{-11} N \qquad (a = 44°)$$
$$F_{9,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((3)+(18) \times 10^{-9})^2} = 0.07 \times 10^{-11} N \qquad (a = 9°)$$
$$F_{10,y} \Rightarrow \frac{23.01 \times 10^{-29}}{(21 \times 10^{-9})^2} = 0.052 \times 10^{-11} N \qquad (a = 49°)$$
$$F_{11,y} \Rightarrow \frac{23.01 \times 10^{-29}}{((18)+(21) \times 10^{-9})^2} = 0.03 \times 10^{-11} N \qquad (a = 40°)$$
$$F_{12,y} \Rightarrow \frac{23.01 \times 10^{-29}}{(3 \times 10^{-9})^2} = 2.56 \times 10^{-11} N$$
$$F_{y_1} \Rightarrow \frac{23.01 \times 10^{-29}}{(40 \times 10^{-9})^2} = 0.014 \times 10^{-11} N$$
$$F_{y_2} \Rightarrow \frac{23.01 \times 10^{-29}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11} N$$
$$F_{ty_3} = (-2.4i, -0.01j) \times 10^{-11} N$$
$$F_{ty} = (1.4i, -3.45j) \times 10^{-11}$$



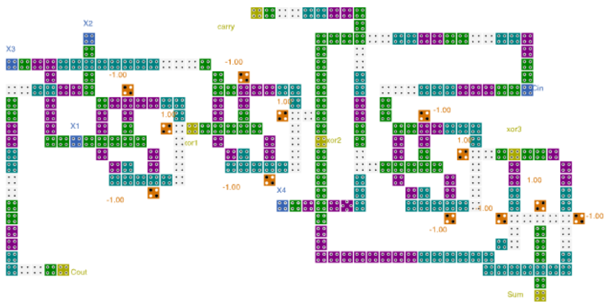
(a) (b)

Figure 8: The resultant of forces from electrons (x,y).

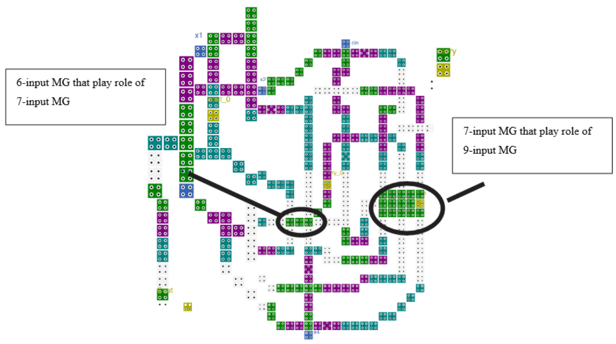
Application: Figure 9 shows the QCA implementation of three designs. Since in the design III we need to duplicate the C_{out} signal, (in order to generate Carry output) the implementation of this theory could be useful. Moreover, to generate the Sum signal the duplication of the C_{out} signal and the duplication of the Carry signal are needed. According to distance concept, when the distance is 2nm, the energy between cells must be 5.76×10^{-9} (Equation (2.7)). In order to reduce the energy to 2.88×10^{-9}, distance is supposed to be 3nm. Therefore, to generate Carry, the C_{out} signal should have 2nm distance with the voter cell. In addition, the C_{out} and Carry signals have 2nm with the voter for generating Sum (see Figure 9c). While the other cells have 3nm distance with the voter cell. In order to design three-input or higher-order Majority circuits, Table 1 is proposed. It is worth to mention that, typically large Majority circuits have approximate performance.



(a) Design I



(b) Design II



(c) Design III

Figure 9: the implementation of design I-III with QCA

Table 1: the number of cell in column and row to implement n-input Majority Function

n-inputn Majority circuit	n-2(column)	n-4 (row)
3	1	0
5	3	1
7	5	3
9	7	5

5. Simulations and results

Simulations have been accomplished with Hspice, QCADesigner, and QCAPro simulators. All designs are simulated with 20nm technology in order to have a fair judgment.
To simulate CMOS and CNT circuits, the technology files of PTM-MG 20nm-nfet and CNFET spice Model are utilized, respectively. The parameters of the Bistable Approximation (only for QCA circuits) is shown in Table 2.

Table 2: The parameters apply to Bistable Approximation by QCADesignert & QCAPro tools

Bistable Option	The value
Number of samples	800000
Convergence tolerance	0.001
Radius of effect	65nm
Relative permittivity	12.9
Clock high	9.8e-0.22
Clock low	3.8e-0.23
Clock shift	0
Clock amplitude factor	2
Layer separation	11.5
Maximum iterations per sample	100
Size of cell	18nm
Y-factor	0.5 EK
Temperature	2

Table 3 shows simulation results related to designs I, II, and III that have been implemented with CMOS, CNT, and QCA. These results describe the power consumption of 4:2 Compressor circuits. Since voltage plays a very significant role in spin devices, these circuits are compared [7]. All results should have the same unit; therefore, they are presented in the Joule unit. Accordingly, SI could be demonstrated:

$$lev = 1.6 \times 10^{-19} J \tag{5.1}$$

$$1Watt = J/S. \tag{5.2}$$

The Equations (5.3,5.4,5.5) show related calculations CMOS, CNT, and QCA respectively. In addition, Table IV compares the new design of QCA with other prototypes in terms of the number of cell, power consumption, area, and clock. These results illustrate in Figure 10.

$$11.13 \times 10^{-9} \times 20 \times 10^{-9} = 22.26 \times 10^{-17} J \tag{5.3}$$
$$9.22 \times 10^{-9} \times 20 \times 10^{-9} = 18.44 \times 10^{-17} J$$
$$5.85 \times 10^{-9} \times 20 \times 10^{-9} = 11.7 \times 10^{-17} J$$
$$8.54 \times 10^{-10} \times 20 \times 10^{-9} = 17.08 \times 10^{-20} J \tag{5.4}$$
$$8.16 \times 10^{-10} \times 20 \times 10^{-9} = 16.32 \times 10^{-20} J$$
$$6.5 \times 10^{-10} \times 20 \times 10^{-9} = 13.5 \times 10^{-20} J$$
$$1.08 \times 10^{-3} \times 1.6 \times 10^{-19} = 1.73 \times 10^{-22} J \tag{5.5}$$
$$0.96 \times 10^{-3} \times 1.6 \times 10^{-19} = 1.54 \times 10^{-22} J$$
$$0.93 \times 10^{-3} \times 1.6 \times 10^{-19} = 1.48 \times 10^{-22} J$$

Table 3: the results of simulation 4:2 Compressors in different architectures with different element in term of power consumption

	CMOS(J)	CNT(J)	QCA(J)
Design I	22.26×10^{-17}	17.08×10^{-20}	1.73×10^{-22}
Design II	18.44×10^{-17}	16.32×10^{-20}	1.54×10^{-22}
Design III	11.7×10^{-17}	13.5×10^{-20}	1.48×10^{-22}

Table 4: The comparison of the new design of QCA with other prototypes

	Cell number	Clock	Area (μm^2)	Power(mev)
Design I	381	12	0.58	1.08
Design II	299	13	0.45	0.96
Design III	297	8	0.36	0.93

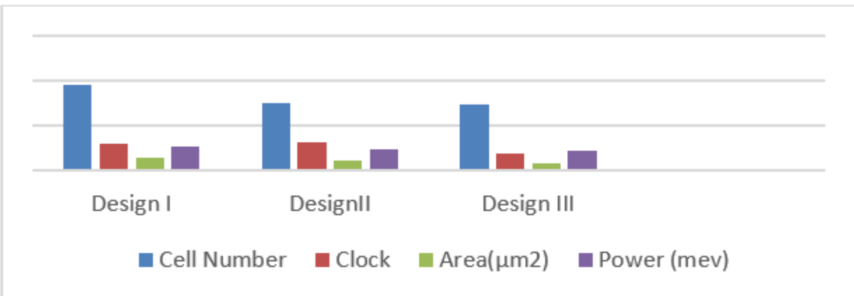


Figure 10: The comparison of 4:2 Compressor in QCA implementation.

6. Conclusion

In this paper, a novel hierarchy is presented to improve digital systems. The 4:2 Compressor is selected as a benchmark to evaluate this hierarchy. In addition, a new implementation of QCA 4:2 Compressor is proposed. According to the results and the evaluations, design III has more acceptable

performance compared to design II. Moreover, design II compared to design I has the same status. In this regard, the power dissipation for these three technologies (CMOS, CNT, and QCA) was in the range of 10^{-17}, 10^{-20} and 10^{-22}, respectively.
In addition, the novel design of QCA 4:2 Compressor has advantages in terms of power consumption as well as area, and speed. We have achieved a significant improvement in terms of cell number, clock, area, and power consumption, $(7.6\%, 23\%, 19\%$ and $5.3\%)$ respectively.

References

[1] Z. Abid, H. El-Razouk and D.A. El-Dib, *Low power multipliers based on new hybrid full Adders*, Micro. J. 39 (2008) 1509–1515.

[2] E. Alkaldy, K. Navi, F. Sharifi and M.H. Moaiyeri, *An ultra-high-speed (4: 2) compressor with a new design approach for nanotechnology based on the multi-input majority function*, J. Comput. Theo. Nano. 11(7) (2014) 1691–1696.

[3] M. Bagherian Khosroshahy, M.Sam Daliri, A. Abdoli, K. Navi and N. Bagherzadeh, *A 3D universal structure based on molecular-QCA and CNT technologies*, J. Molec. Struc. 1119 (2016) 86–95.

[4] B.K. Bhoi, T. Das, N.K. Misra and R. Rout, *An explicit cell-based nesting robust architecture and analysis of full adder*, Paper presented at the Recent Trends in Communication, Computing, and Electronics, Singapore, 2019.

[5] C.-H. Chang, J. Gu and M. Zhang, *Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits*, IEEE Transactions on Circuits and Systems I: Regular Papers 51, 1985-1997 Institute of Electrical and Electronics Engineers (IEEE), 2004.

[6] L. Dadda, *Some schemes for fast serial input multipliers*, In 1983 IEEE 6th Symposium on Computer Arithmetic (ARITH). IEEE, 1983.

[7] E. Dmitri Nikonov and I. A. Young, *Benchmarking of beyond-CMOS eyploratory devices for logic integrated circuits*, IEEE Journal on Eyploratory Solid-State Computational Devices and Circuits 1, 3–11 Institute of Electrical and Electronics Engineers (IEEE), 2015.

[8] P. Douglas Tougaw and C. S. Lent, *Logical devices implemented using quantum cellular automata*, J. Appl. Phys. 75 (1994) 1818–1825.

[9] R. Farazkish, F. Khodaparast, K. Navi and A. Jalali, *Design and characterization of a novel inverter for nano-electronic circuits*, Proc. Int. Conf. Nanotech. Fund. Appl. pp. 4-6 August 2010.

[10] J. Gu and C.-H. Chang, *Ultra low voltage low power 4-2 compressor for high speed multiplications*, Proc. 2003 Int. Symp. Circ. Syst. IEEE, 2003.

[11] G.M. Howard, P. Mokrian, M. Ahmadi and W.C. Miller, *Power and Delay Analysis of 4:2 Compressor Cells*, In 2005 IEEE International Symposium on Circuits and Systems. IEEE, 2005.

[12] D. Jacobsohn, *A suggestion for a fast multiplier*, IEEE Trans. Elect. Comput. EC-13, Instit. Elect. Elect. Engin. (IEEE), (1964) 754–754.

[13] M.J. Kelly *Nano Manufacturing for Electronics or Optoelectronics*, In Future Trends in Microelectronics, 2016.

[14] P. Keshavarzian and K. Navi, *Optimum quaternary Galois field circuit design through carbon nano tube technology*, In 15th International Conference on Advanced Computing and Communications (ADCOM 2007), IEEE, 2007.

[15] I. Koren, *Computer Arithmetic Algorithms Second Edition*, A K Peters/CRC Press, 2001.

[16] P. Mokrian, G.M. Howard, G. Jullien and M. Ahmadi, *On the use of 4:2 compressors for partial product reduction*, In CCECE 2003 - Canadian Conference on Electrical and Computer Engineering. Toward a Caring and Humane Technology (Cat. No.03CH37436), IEEE, 2003.

[17] N. Mousavi and S. Gorgin, *The novel architecture for 4:2 compressors*, CSCCIT Conf. 2011.

[18] N. Moosavi, K. Navi and V. Aghazarian, *Ultra-low cost full adder cell using the nonlinear effect in four-input quantum dot cellular automata majority gate*, Int. J. Nonlinear Anal. Appl. 11(2) (2008) 1–16.

[19] K. Prasad and K.K. Parhi,*Low-power 4-2 and 5-2 compressors*, In Conference Record of Thirty-Fifth Asilomar Conference on Signals Systems and Computers (Cat.No.01CH37256), IEEE, 2001.

[20] J.M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits (A design perspective)*, Prentice Hall, 2003.

[21] D. Radhakrishnan and A.P. Preethy, *Low power CMOS pass logic 4-2 compressor for high-speed multiplication*, In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (Cat.No.CH37144), IEEE, 2000.

[22] S. Seyedi and N. Jafari Navimipour, *An optimized design of full Adder based on nanoscale quantum-dot cellular automata*, Optik 158 (2018) 243–256.

[23] A.M. Shams and M.A. Bayoumi, *A structured approach for designing low power adders*, Conf. Record Thirty-First Asilomar Conf. Sign. Syst. Comput. IEEE Comput. Soc, 1997.

[24] E. E. Swartzlander, H. Cho, I. Kong and S.-W. Kim, *Computer arithmetic implemented with QCA: A progress report*, In 2010 Conference Record of the Forty Fourth Asilomar Conference on Signals Systems and Computers, IEEE, 2010.

[25] S. Veeramachaneni, K. Krishna, L. Avinash, S. Puppala and M.B. Srinivas, *Novel architectures for high-speed and low-power 3-2 4-2 and 5-2 compressors*, 20th Int. Conf. VLSI Design held jointly with 6th Int. Conf. Embedded Syst. IEEE, 2007.

[26] M. Weinan and L. Shuguo, *A new high compression compressor for large multiplier* In 2008 9th International Conference on Solid-State and Integrated-Circuit Technology,IEEE, 2008.

[27] R. Zimmermann and W. Fichtner, *Low-power logic styles: CMOS versus pass-transistor logic*, IEEE J. Solid-State Circ. Instit. Elect. Elect. Engin. 32 (1997) 1079–1090.