



# Ultra-Low Cost Full Adder Cell Using the nonlinear effect in Four-Input Quantum Dot Cellular Automata Majority Gate

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## Abstract

In this article, a new approach for the efficient design of quantum-dot cellular automata (QCA) circuits is introduced. The main advantages of the proposed idea are the reduced number of QCA cells as well as increased speed, reduced power dissipation and improved cell area. In many cases, one needs to double the effect of a particular inter median signal. State-of-the-art designs utilize a kind of fan out to achieve these resulting in increased number of cells, dissipating more power and decreasing the overall speed of the circuits. In this paper, we have presented cell alignment to multiply the effect of a certain signal by two, three or even more. This can be considered as a new vision to design any arbitrary circuit needing this property. Furthermore, a new coplanar crossover approach has been introduced which is able to make the coplanar crossover in two consecutive clocks with one rotated cell in the worst case. In order to prove the efficiency of the proposed ideas, a new Full Adder cell and a new Carry Ripple Adder (4-bit) have been designed which provides less QCA cell count as well as less power dissipation and cost.

*Keywords:* Quantum Dot Cellular, Distance, Coplanar Crossover, Full Adder.

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## 1. Introduction

Nowadays, researchers are seeking new alternative approaches for complementary metal oxide semiconductor (CMOS). Among these technologies, quantum-dot cellular automata (QCA) is a novel phenomenon that possesses unique characteristics such as ultra-low power consumption, high speed, and low area [1-2]. In this technology, logic states are not based on the voltage or current levels. In other words, the position of electrons creates the required polarization. The polarization indicates the level of distributed charge in the direction of the diagonal axis ( $P = +1, P = 0$ ). Therefore, all binary circuits can be designed by QCA [3-4]. The arithmetic circuits such as subtractor, adder, divider, multiplier and some sequential circuits like flip-flops are examples of these studies [5-6]. Moreover, additional works on random access memory cells and counters have been carried out [7]. Meanwhile, adder circuits are the most common area of research and any substantial improvements for this component will affect the whole system.

Hitherto, four methods of the QCA implementation have been suggested; magnetic [2-8], metal island [9], molecular QCA [10] and semiconductor [11]. The main idea of this research is to propose a new method for low cost and low complexity QCA design. The electrical field can be modified by increasing or decreasing the distance of the neighbor cells. This method can be utilized instead of multiplying the signal by two. In addition, one novel technique of coplanar crossover has been presented. In order to verify the accuracy and evaluate the scalability of these ideas, one Full Adder (FA) cell and a Carry Ripple Adder (CRA) were designed.

The rest of this paper is organized as follows. In Section 2 basic theory in QCA domain is discussed. State-of-the-art adders and proposed ideas are discussed in sections 3 and 4, respectively. Subsequently, the performance evaluation of the proposed designs is presented in section 5. Finally, section 6 presents the conclusion.

## 2. QCA Background

### 2.1. Fundamental Structures

The primary element in QCA design is a cell with two mobile electrons (Figure 1a). In this technique, logical states are defined based on the position of electrons in the cell (polarization), not voltage level [12]. Majority gate and inverter gate are the basic elements in QCA circuit design. The logical function of a three-input majority gate (Figure 1b) is as follows:

$$Maj(A, B, c) = AB + Bc + Ac \quad (2.1)$$

In order to implement 2-input “AND” and “OR” logic gates, we just need to modify a polarization of one of the inputs in Equation 1. That is, it can be set to -1 (logic 0) and 1 (logic 1), respectively. Equations 2 and 3 show these concepts. In addition, in Figure 2 some common inverters have been illustrated [13].

$$Maj(A, B, 0) = AB + A(0) + B(0) = AB \quad (2.2)$$

$$Maj(A, B, 1) = AB + A(1) + B(1) = A + B \quad (2.3)$$

The Coulomb force between two cells  $i$  and  $j$  is expressed in Equation 4. In fact, with calculating all charges around the cell, electrostatic interactions (forces) can be illustrated. Each electron in cell  $i$ , possesses the electrostatic interaction with another electron in its neighbor (cell  $j$ ) and it is calculated as follows [15-16]:

$$F_{i,j} = K \frac{q_i q_j}{r^2} \quad (2.4)$$

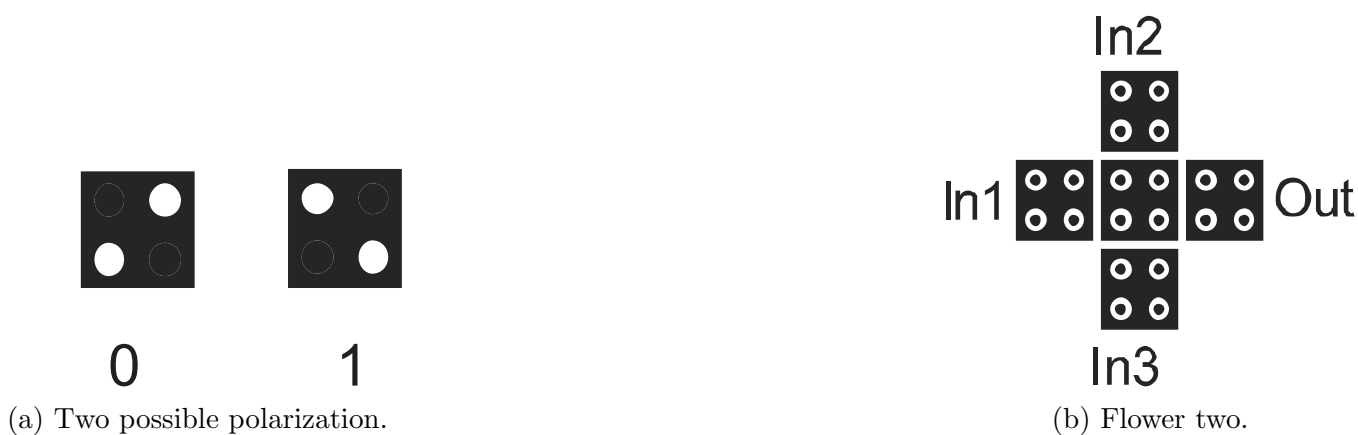


Figure 1: Basic logic cells and design in QCA

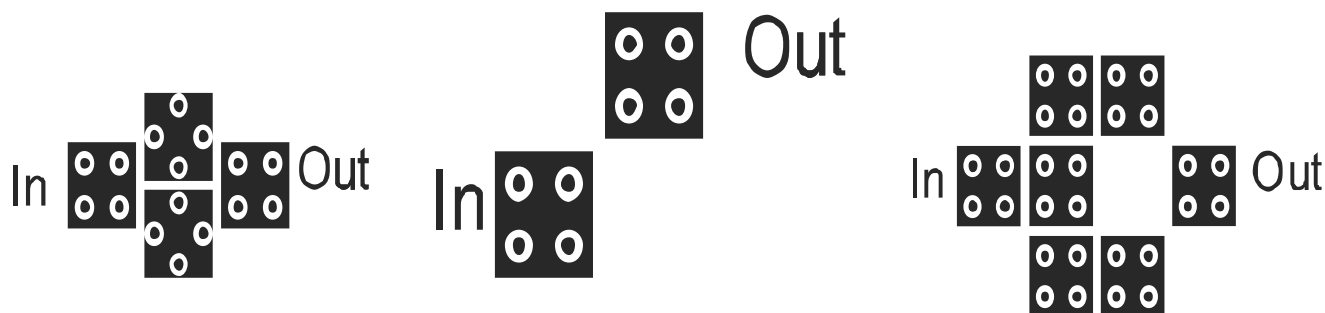


Figure 2: Common Inverters in QCA.

In Equation 4,  $K$  is Coulomb's constant also  $q_{i-j}$  and  $r$  exhibit amounts of electron and the distance between cells, respectively.

### 2.2. QCA Clocking

Landauer hypothesis is currently being used to schedule the timing of the system. According to this concept, each clock signal is divided into four parts (Figure 3a) [17]. These four phases are Switch, Hold, Release and Relax. Indeed, during each of the phases, there is an operation that will be discussed.

In Switch Phase the electrons are polarized under the influence of neighboring cells. The first part of Figure 3b show this concept (left-side). In Hold phase the inter-dot barriers are increased; therefore, electrons do not turn to the previous phase (the second part of Figure 3b). Release phase: Inter-dot barriers are decreased and the cell changes into the unpolarized state (the third part of Figure 3b). Relax phase: there are no inter-dot barriers so the cells are not influenced by the polarity of the neighbor cells (the fourth part of Figure 3b) [13].

In QCA circuits, as well as most digital circuits, the clocking signal is needed for several reasons. First, the clock signal is the sole solution to control timing in QCA circuits. The current flow does not exist in QCA circuits. Hence, information flow control is required which can be done by setting clock from inputs to the outputs. Second, a pipeline mechanism should be established in QCA circuits. In order to avoid the KINK state, it is required to utilize multiple clocks. In this situation, a large number of cells are changed or switched at the same time. Furthermore, it preserves the circuit in a ground state [18-20].

### 2.3. Power Consumption Analysis

The consumption of adiabatically power dissipation of a QCA cell is computed by a Hamiltonian matrix. The Hamiltonian and the Coulomb interaction are described utilizing Hartree-Fock approximation of cells in Equation 5:

$$H = \begin{bmatrix} -E_k/2 \sum C_i f_{i,j} & -\gamma \\ -\gamma & E_k/2 \sum C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} -E_k/2(C_{j-1} + C_{j+1}) & -\gamma \\ -\gamma & E_k/2(C_{j-1} + C_{j+1}) \end{bmatrix} \quad (2.5)$$

Where  $C_i$  describes the polarization of the  $i_{th}$  side of the cell.  $f_{i,j}$  is the geometrical character of electrostatic interaction between  $i$  and  $j$  cells regarding their geometrical distance.  $\gamma$  stand for tunneling energy between cells (two states). The Kink energy ( $E_k$ ) is demonstrated as Equation 6:

$$E_{i,j} = \frac{1}{4 \prod \epsilon_0 \epsilon_r} \sum_{n=1}^4 \sum_{m=1}^4 \frac{q_{i,n} q_{j,m}}{|r_{i,n} - r_{j,m}|} \quad (2.6)$$

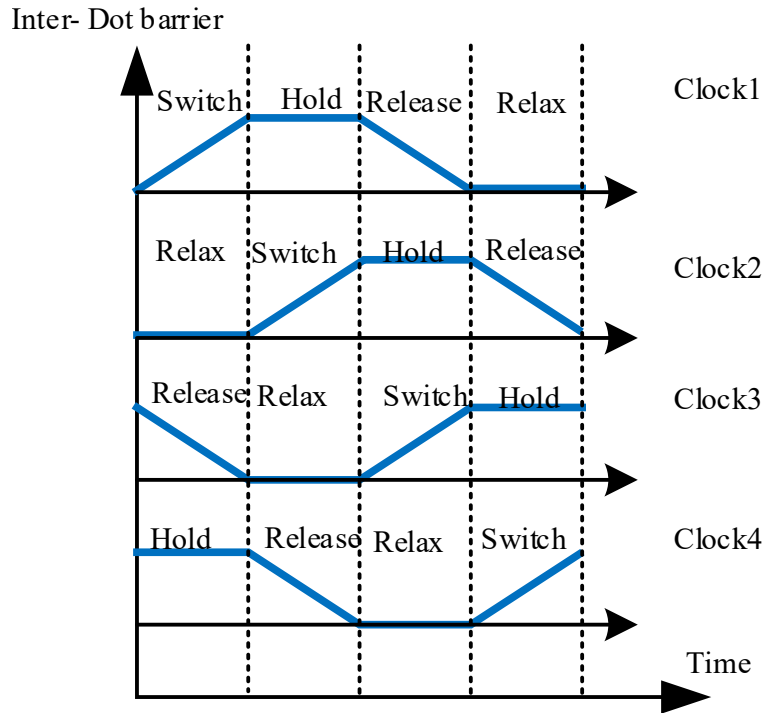
The amount of a quantum-dot cell energy at every clock cycle is as:

$$E = \langle H \rangle = \frac{\hbar}{2} \vec{\lambda} \vec{\Gamma} \quad (2.7)$$

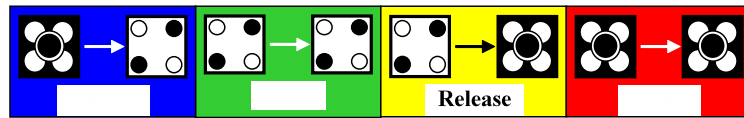
$\vec{\lambda}$  is the coherence vector,  $\hbar$  expresses diminished Planck constant and  $\vec{\Gamma}$  is the energy environment vector of the cell (three-dimensional). It is presented as:

$$\vec{\Gamma} = \frac{1}{\hbar} [-2\gamma, 0, E_k (C_{j-1} + C_{j+1})] \quad (2.8)$$

In the above Equation, the  $(C_{j-1} + C_{j+1})$  shows the summation of neighbor polarizations. The energy and power consumption are related to each other as shown in Equation 9. This means that



(a) Landauer Clock waveform [17]



(b) One clock period in QCA [19].

Figure 3

the power consumption is calculated by the derivative of the energy with respect to time. The power consumption of a QCA cell is divided into four major branches (Equation 10). The  $P_{in}$  is power consumption from the left adjacent QCA cell.  $P_{out}$  is related to power consumption of the right side cell. In the process of Switch phase, inter-dot obstacles continuously generate transmission energy ( $P_{clock}$ ). Finally, there is insignificant power dissipation ( $P_{bath}$ ). These Equations, for the single QCA cell, have been demonstrated in (11-14) [21-24]:

$$\frac{dE}{dt} = P^f(t) \quad (2.9)$$

$$P^f = P_{in} - P_{out} + P_{clock} - P_{bath} = 0 \quad (2.10)$$

$$P_{in} = \frac{1}{T_c} \int_t^{t+T_c} \frac{\hbar E_K}{2} \frac{dP_L(\dot{t})}{d\dot{t}} \lambda_3(\dot{t}) dt \quad (2.11)$$

$$P_{out} = -\frac{1}{T_c} \int_t^{t+T_c} \frac{\hbar E_K}{2} \frac{dP_R(\dot{t})}{d\dot{t}} \lambda_3(\dot{t}) dt \quad (2.12)$$

$$P_{clock} = \frac{1}{T_c} \int_t^{t+T_c} \frac{\hbar}{2} \frac{d\Gamma_1(\dot{t})}{d\dot{t}} \lambda_1(\dot{t}) dt \quad (2.13)$$

$$P_{bath} = \frac{\hbar}{2\tau T_c} \int_t^{t+T_c} \{ \lambda_1(\dot{t}) \Gamma_1(\dot{t}) + \lambda_3(\dot{t}) \Gamma_3(\dot{t}) + \tanh[\Delta(\dot{t})] \sqrt{\Gamma_1(\dot{t})^2 + \Gamma_3(\dot{t})^2} \} dt \quad (2.14)$$

### 3. State Of The Art Adders

Since a large amount of operations in the computer arithmetic have been carried out by adding operator, it plays a significant role in this area. Moreover, their performance could affect the whole system significantly. Traditionally, the one-bit Full Adder possesses three inputs (A, B, and  $C_{in}$ ) with two outputs (Sum and  $C_{out}$ ) as follows:

$$Sum = A \oplus B \oplus C_{in} \quad (3.1)$$

$$C_{out} = AB + AC_{in} + BC_{in} \quad (3.2)$$

Three-input majority gate could generate the Carry output ( $C_{out}$ ). One of the major aims of FA designers is to eliminate the slow and power consuming three input XOR gates. This issue made researchers offer suitable designs and hybrid cells for Full Adders just by utilizing majority gates. In the first version majority function was used to create the Full Adder with five majority gates and three inverter gates (Figure 4a) [13]. The next improved approach is exhibited in Figure 4b [25]. It is composed of two inverters and three majority gates. According to this approach, several QCA implementations were designed [26-27]. In this process, the other Full Adder structure is shown by [28] (Figure 4c). It is an expression of five-input majority gate. This design has a five-input majority, a three-input majority, and an inverter gate.

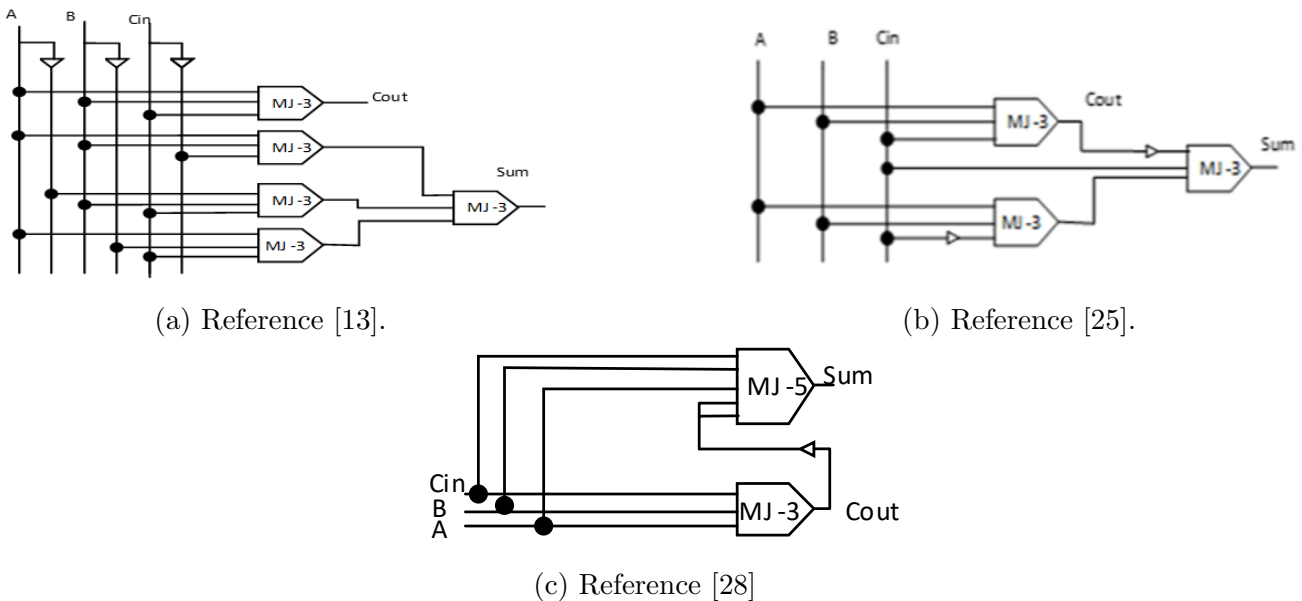


Figure 4: Full Adders

In this regards, three-input and five-input majority functions have been used to design these circuits. Some types of layouts for a five-input majority function have been illustrated in Figure 5. These types have been designed with 10 cells, 18 cells and 33 cells in [28-30], respectively.

### 4. Proposed Ideas

#### 4.1. Proposed Crossover

**Approach:** The transfer of information is in the Switching phase of the clock and from the next phase the signal will be entered in the latch state (when it starts the signal locking process) [18-19].

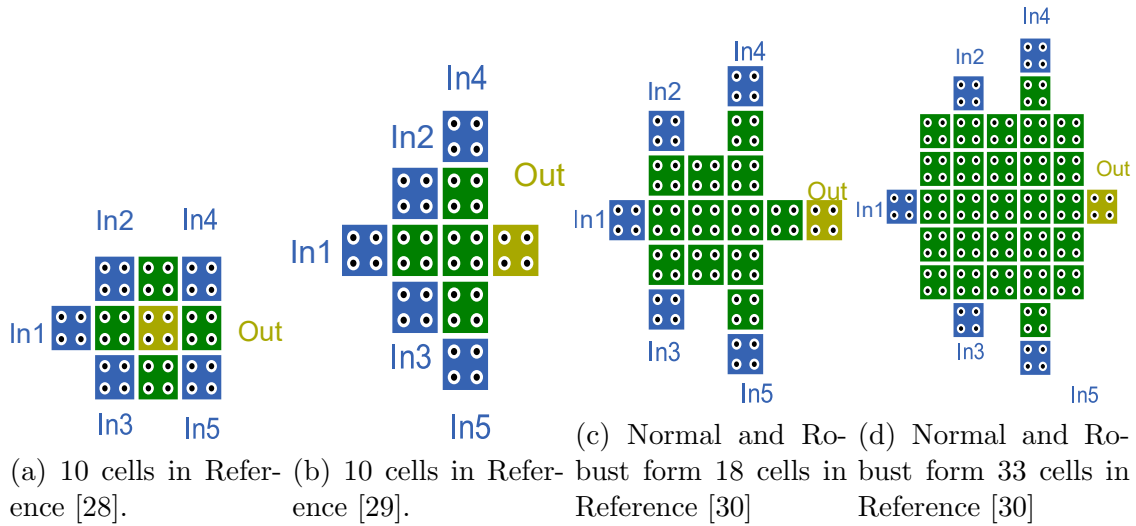


Figure 5: Four types of layout for a five-input majority function.

Therefore, using this  $\pi/2$  phase difference between two consecutive clocks makes the safe crossovering of two arbitrary signals. Moreover, clocking method in QCA has pipeline behavior. In other words, the cells are in a stable state and it will happen when the cell is not influenced by the polarity of the neighbor cells; which is a combination of Release and Relax modes. Considering the Hold phase, as the first phase of the locking process, noise can be created in the cross point of the signals. We have found out that eliminating just one cell (in small circuits) or rotating it (in large circuits) will resolve this problem. In this method, only one rotated cell exists while in [13], a series of rotated cells are used (see Figure 6a). Besides, the fact that our crossing method utilizes two consecutive clocks, result in decreasing the number of clock phases compared to [31-32] (Figure 6b).

**Application:** In Figure 6c the proposed coplanar crossover has shown. It could make the coplanar crossover in two consecutive clocks. This type is suitable to employ in small circuits. In fact, the second cell after traversing crossover is eliminated. In large circuits, this cell is rotated (Figure 6d). Figure 6e shows the crossed and inverted cells at the same time. Finally, Figure 6f and Figure 6g have illustrated that the second phase crossovers the third phase of the clock and the third phase crossovers the next phase of the clock, respectively.

#### 4.2. Proposed Distance Theory

**Approach:** When it is necessary to double the effect of signal, Equation 4 can be used to obtain the required force. It should be noted that the force and distance of the electrons have opposite relation. Reducing the distance between intercellular (less than 2nm) is contrary to the rules of technology so this goal can be implemented by reducing the force. In other words, when the double effect of the signal is needed, the distance is in its default state and when the effect of signal does not need to be increased the distance is increased; as a result, the force will be reduced. Based on this approach we have implemented a new Full Adder cell.

**Application:** First, using a three-input majority gate with A, B, and  $C_{in}$  inputs, the Carry ( $C_{out}$ ) is generated (Equation 17). Then, to calculate the Sum signal, a four-input majority gate is needed in which the Carry signal has the default distance of 2nm from the voter cell whereas the distance between the other inputs (A, B, and  $C_{in}$ ) is 3nm (Figure 7a). This structure implements a four-input majority function which is able to generate the Sum output (Equation 18). According to Equation 4 when the distance is 2nm, the force between cells must be  $5.76 \times 10^{-11}$  (Equation 19). In order to

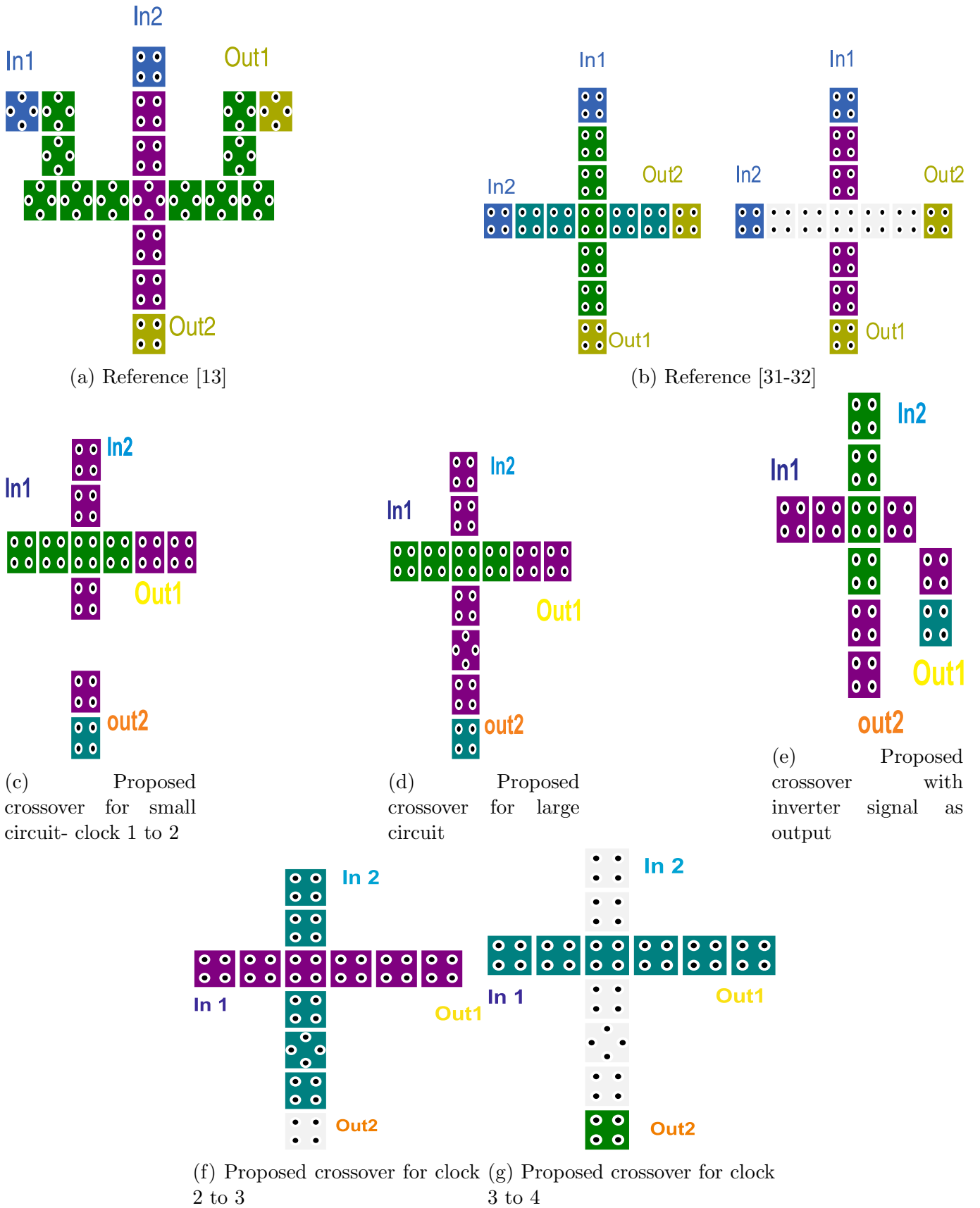


Figure 6: Coplanar crossover



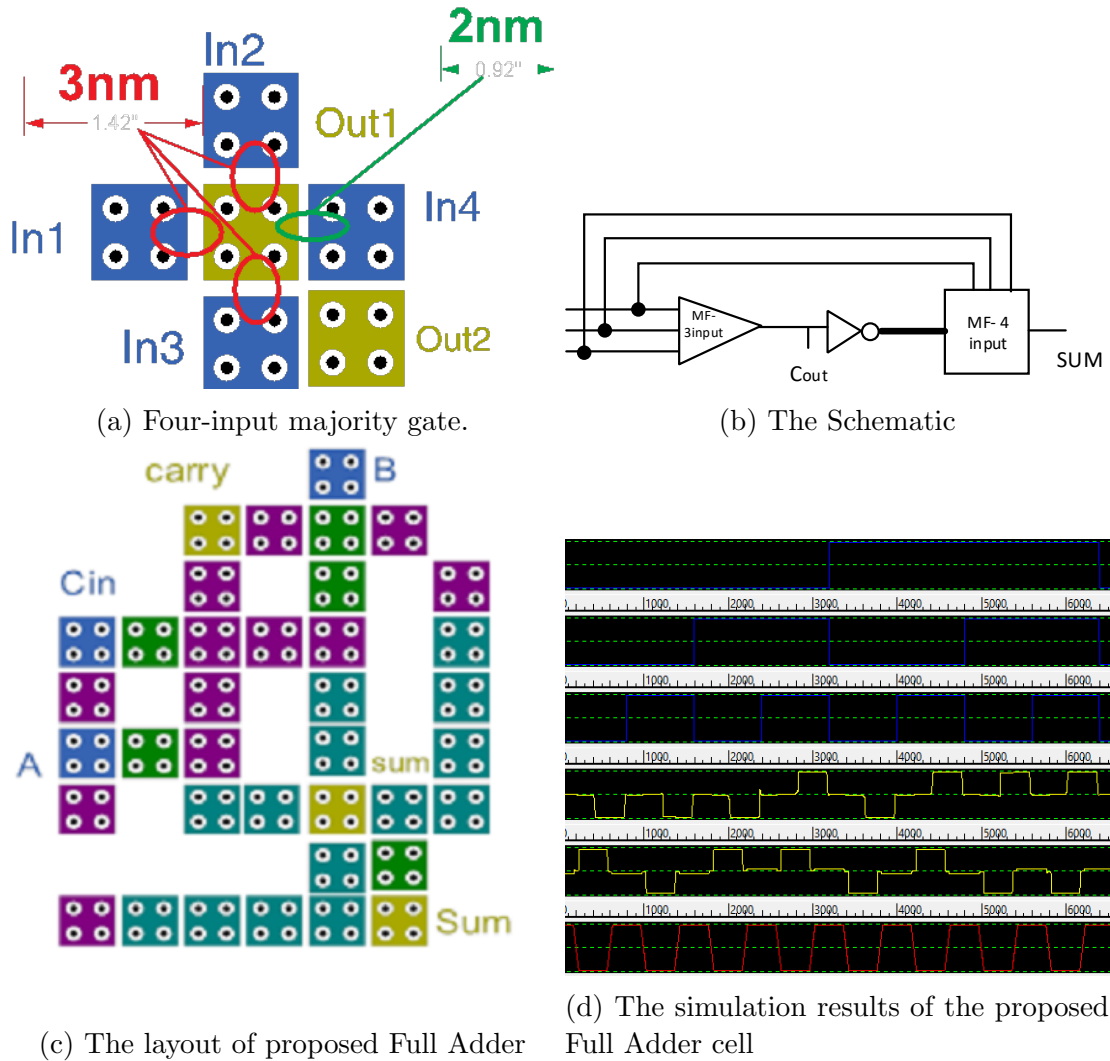


Figure 7

reduce the energy to  $2.88 \times 10^{-11}$ , distance is supposed to be 3nm (Equations 20-21). The schematic layout as well as simulation results of the proposed Full Adder cell have been shown in Figure 7b, Figure 7c, and Figure 7d, respectively. It worth to mention that, the proposed Full Adder has utilized the proposed crossover.

$$C_{out} = Maj(A, B, C_{in}) \tag{4.1}$$

$$Sum = Maj(A, B, C_{in}, \overline{C_{out}}, \overline{C_{out}}) \tag{4.2}$$

$$F_{i,j} = K \frac{q_i q_j}{r^2} = > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(2 \times 10^{-9})^2} = 5.76 \times 10^{-11} N \tag{4.3}$$

$$\frac{1}{2} F_{i,j} = K \frac{q_i q_j}{r^2} = > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{X^2} = 2.88 \times 10^{-11} N \tag{4.4}$$

$$X = 2.82 \times 10^{-9} \cong 3nm \tag{4.5}$$

**Physical Proof:** Equations (22-25) and Figure 8 show the effective force between electrons. These calculations prove that the proposed structure is correct and has the output for five-input majority

function. Since the calculations are the same in each state, only one of the critical states has been calculated.

**State (“1100”), electron x, (see Figure 8a):**

$$\begin{aligned}
 F_{1,x} &= K \frac{q_i q_j}{r^2} = > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 21) \times 10^{-9})^2} = 0.03 \times 10^{-11} \text{N} (\alpha = 41^\circ) \\
 F_{2,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(3 \times 10^{-9})^2} = 2.55 \times 10^{-11} \text{N} \\
 F_{3,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(39 \times 10^{-9})^2} = 0.015 \times 10^{-11} \text{N} \\
 F_{4,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 21) \times 10^{-9})^2} = 0.03 \times 10^{-11} \text{N} (\alpha = 41^\circ) \\
 F_{5,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 39) \times 10^{-9})^2} = 0.013 \times 10^{-11} \text{N} (\alpha = 65^\circ) \\
 F_{6,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(21 \times 10^{-9})^2} = 0.052 \times 10^{-11} \text{N} \\
 F_{7,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 2) \times 10^{-9})^2} = 0.070 \times 10^{-11} \text{N} (\alpha = 84^\circ) \\
 F_{8,x} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11} \text{N}
 \end{aligned} \tag{4.6}$$

$$\sum_{i=1}^8 F_{i,x} = 2.44 \times 10^{-11} \text{N} \tag{4.7}$$

**State (“1100”), electron y, (see Figure 8b):**

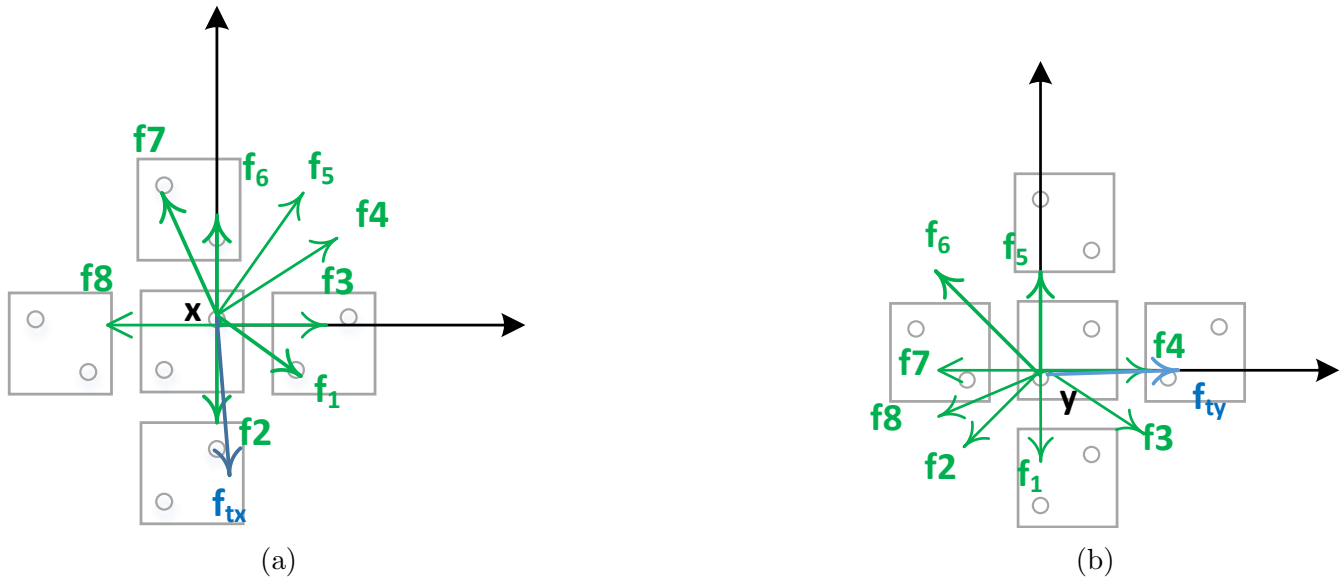


Figure 8: The resultant of forces from electrons (x,y).

$$\begin{aligned}
 F_{1,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(39 \times 10^{-9})^2} = 0.015 \times 10^{-11} \text{N} \\
 F_{2,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 21) \times 10^{-9})^2} = 0.03 \times 10^{-11} \text{N} (\alpha = 49^\circ) \\
 F_{3,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 21) \times 10^{-9})^2} = 0.03 \times 10^{-11} \text{N} (\alpha = 41^\circ) \\
 F_{4,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(3 \times 10^{-9})^2} = 2.55 \times 10^{-11} \text{N} \\
 F_{5,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(21 \times 10^{-9})^2} = 0.052 \times 10^{-11} \text{N} \\
 F_{6,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 3) \times 10^{-9})^2} = 0.069 \times 10^{-11} \text{N} (\alpha = 9^\circ) \\
 F_{7,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{(20 \times 10^{-9})^2} = 0.057 \times 10^{-11} \text{N} \\
 F_{8,y} &= > \frac{8.99 \times 10^9 \times 2.56 \times 10^{-38}}{((18 + 38) \times 10^{-9})^2} = 0.013 \times 10^{-11} \text{N} (\alpha = 25^\circ) \\
 \sum_{i=1}^8 F_{i,y} &= 2.4 \times 10^{-11} \text{N}
 \end{aligned} \tag{4.8}$$

$$\sum_{i=1}^8 F_{i,y} = 2.4 \times 10^{-11} \text{N} \tag{4.9}$$

## 5. Performance Evaluation & Comparisons

We have investigated the effectiveness of the proposed ideas. Consequently, the new Full Adder and the previous relevant designs was simulated via the conventional tools. The QCADesigner version

Table 1: The detailed comparison of the proposed one-bit Full Adder cells.

Name	# cell	Area ( $\mu\text{m}^2$ )	Clock	Power (me V)	Complexity (cost)
[34]	292	626.7	$3\frac{2}{4}$	—	$(5^2 + 0 + 8^2) \times 3\frac{2}{4} = 311.5$
[25]	145	157.2	$1\frac{1}{4}$	451	$(3^2 + 2 + 6^2) \times 1\frac{1}{4} = 58.75$
[35]	131	149.6	2	502	$(3^2 + 2 + 3^2) \times 2 = 40$
[36]	123	160.0	$1\frac{1}{4}$	520	$(3^2 + 2 + 3^2) \times 1.25 = 25$
[37.1]	124	124.1	$1\frac{3}{4}$	445	$(3^2 + 4 + 4^2) \times 1\frac{3}{4} = 50.75$
[38]	113	105	1	587	$(2^2 + 2 + 3^2) \times 1 = 15$
[39]	102	98.35	2	282	$(3^2 + 2 + 3^2) \times 2 = 40$
[37.2]	95	96.29	$1\frac{1}{4}$	408	$(2^2 + 2 + 2^2) \times 1\frac{1}{4} = 12.5$
[40]	95	90.25	2	378	$(2^2 + 1 + 0) \times 2 = 10$
[41]	87	73.68	1	—	$(3^2 + 2 + 2^2) \times 1 = 15$
[42]	71	57.11	$1\frac{2}{4}$	304	$(2^2 + 2 + 2^2) \times 1\frac{2}{4} = 15$
[43]	69	82.04	1	330	$(4^2 + 6 + 2^2) \times 1 = 26$
[44]	59	42.36	1	237	$(3^2 + 2 + 2^2) \times 1 = 15$
[45]	53	54.64	$\frac{3}{4}$	205	$(2^2 + 6 + 2^2) \times \frac{3}{4} = 10.5$
[46]	46	56.15	1	—	$(2^2 + 4 + 2^2) \times 1 = 12$
Proposed	37	24.97	1	177	$(2^2 + 1 + 2^2) \times 1 = 9$

2.0.3 (Bistable Approximation with default parameters except number of sample=1000000 in terms of CRA) and QCAPro (with temperature 2, Y-factor 0.5EK) simulators were utilized for these simulations. All designs are evaluated via the benchmark of [33]. Table I shows the comparison of Full Adders. The QCAPro does not show the result for some cases so these cases have been indicated with dash sign in table. Equation 26 is the evaluation benchmark that is mentioned in [33] where M, I, and, C are the number of majority gate, inverter, and crossover, respectively, and T indicates clocking time.

The coefficients (K, l, and p) indicate the importance of power dissipation, complexity, and latency where k=l= 2 and p=1 have been selected in [33].

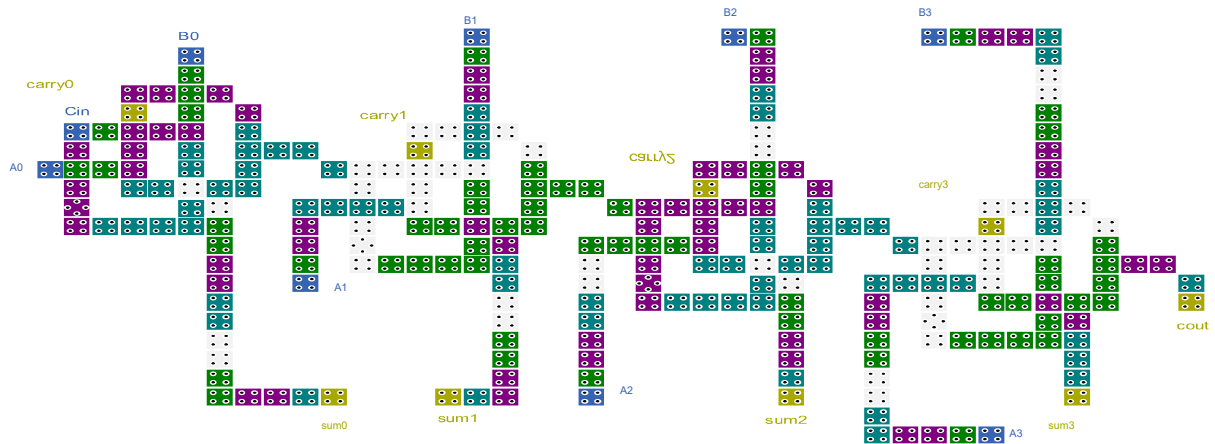
$$C_{cost} = (M^k + I + C^l)Tp \quad (5.1)$$

Table II compares the results of some examples using our proposed design with previous Carry Ripple Adder (4-bit). Some pervious Carry Ripple Adders are not mentioned in Table II because at least one of their inputs or outputs is not available in cell implementation.

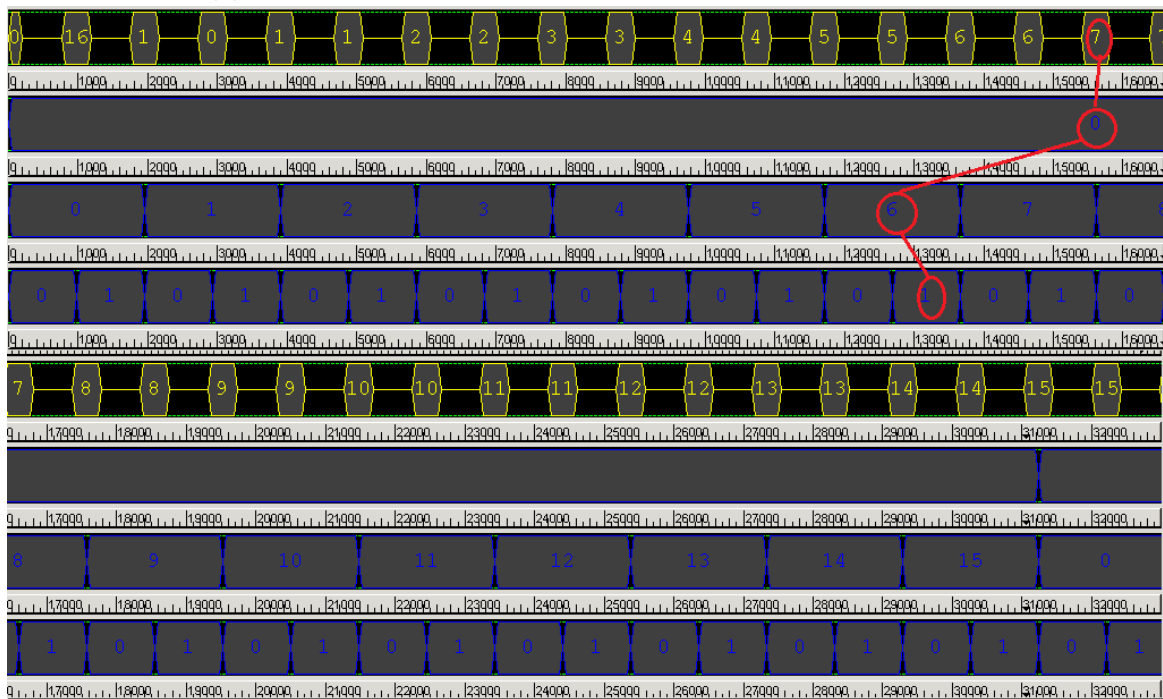
In Figure 9a the proposed 4-bit Carry Ripple Adder is illustrated. In Figure 9b the final waveforms of simulation using our 4-bit Carry Ripple Adder is shown. For example, decimal numbers 0, 6, and 1 are assigned to  $(a_3 a_2 a_1 a_0)$ ,  $(b_3 b_2 b_1 b_0)$  and  $C_{in}$ , respectively. The result is equal to 7 which is shown by  $(C_{out} S_3 S_2 S_1 S_0)$ . Following the same approach, we have provided Figure 10 that depicts table I and II.

## 6. Conclusion

In this paper, a novel method is proposed in order to double the signal effect. In addition, one type of coplanar crossover is presented with one clock less in comparison to state-of-the-art. The proposed ideas resulted in designing new enhanced one bit Full Adder cell and CRA (4-bit). Three-input and four-input majority functions are used in this new design in which the Four-input majority function is an alternative approach to the five-input majority function based on our distance concept.



(a) 4-bit Carry Ripple Adder with the proposed Full Adder

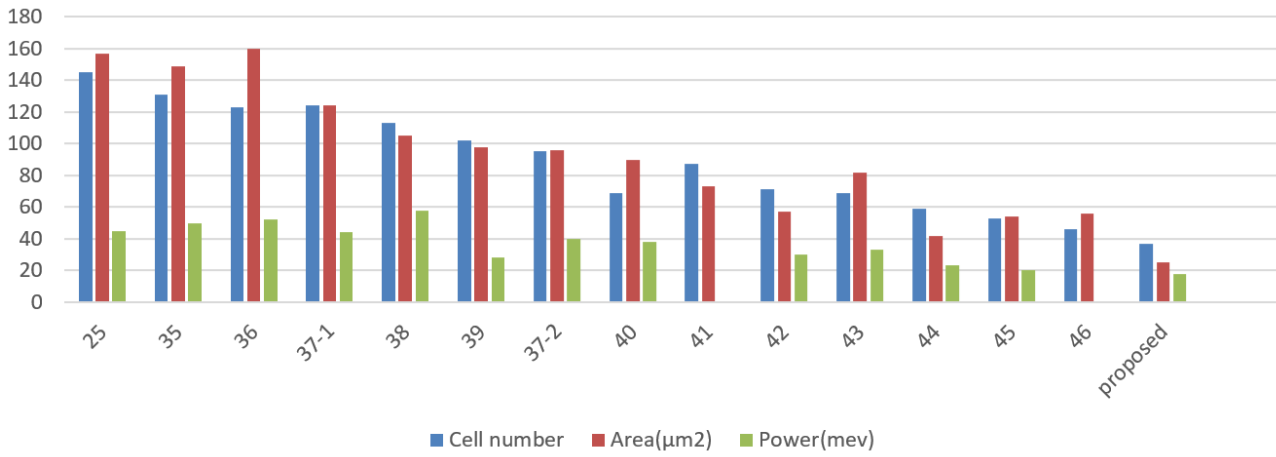


(b) The simulation results of the 4-bit CRA.

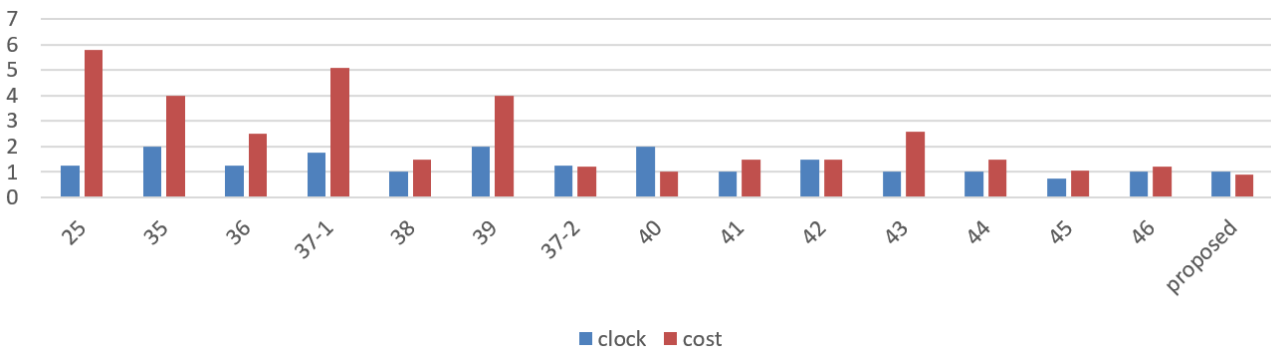
Figure 9

Table 2: Detailed comparison of the proposed 4-bit CRA with same structures.

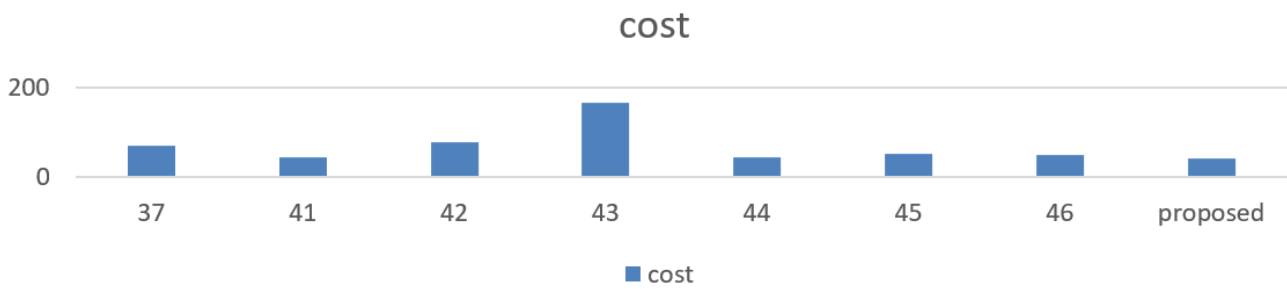
Name	# cell	Clock	Complexity
[37]	401	17	$4 \times [(2^2 + 2 + 2^2)] \times 17 = 680$
[41]	373	7	$4 \times [(3^2 + 2 + 2^2)] \times 7 = 420$
[42]	442	19	$4 \times [(2^2 + 2 + 2^2)] \times 19 = 760$
[43]	411	16	$4 \times [(4^2 + 6 + 2^2)] \times 16 = 1664$
[44]	258	7	$4 \times [(3^2 + 2 + 2^2)] \times 7 = 420$
[45]	281	9	$4 \times [(2^2 + 6 + 2^2)] \times 9 = 504$
[46]	283	10	$4 \times [(2^2 + 4 + 2^2)] \times 10 = 480$
Proposed	250	10	$4 \times [(2^2 + 2 + 2^2)] \times 10 = 400$



(a) The number of cells, Area and Power of Full Adders



(b) The clock and cost of Full Adders



(c) The Cost of 4-bit CRA

Figure 10: The result charts

To evaluate the proposed designs, several coplanar Full Adders are chosen and compared. These evaluations have utilized QCADesigner and QCAPro as simulators and evaluation benchmark in [33]. Based on the analysis, the proposed Full Adder has 24 percent less complexity (in the Full Adder terms) and 12.5 percent less complexity (in the CRA) compared to the best designs.

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