A comparative study of two types of substrates in the manufacture of Schottky diode: p-Si and n- Si

Hussam Muhsin Hwail[a,*], Manal Midhat[b]

[a]*Department of Physics, University of Kufa, Najaf,Iraq.*
[b]*Department of Physics, University of Baghdad, Al-Jadria, Baghdad, Iraq.*

(Communicated by Madjid Eshaghi Gordji)

Abstract

This paper includes description of fabrication and characterization of two Schottky diodes differ in substrate material (n-type and p-type black Silicon). Schottky diodes were composed of (Ag /B-Si/n-Si/Al and Ag/B-Si/p-Si/ Al) respectively. Etching was achieved both electrochemical and photo–electrochemical etching processes. Different etching times and etching current densities were applied. Ag for front contact and Al for back contact were deposited by thermal evaporation method. I-V characteristics were plotted for the diode in dark forward and backward biasing at room temperature. The ideality factor and barrier height values were obtained. The barrier height values was(0,33-0,36) eV and the saturation current values (6,86-7,05) for the diode samples were obtained from the current-voltage (I-V) curves , The ideality factor (n) values was(27.47-35.61), Schottky diodes at the Ag/BS or the dual metal-semiconductor junctions (Ag/BS/c-Si and c- Si/Al), of a diode ideally exhibit Ohmic features).

Keywords: Mathematics,Black Silicon, schottky diode, Electrochemical Etching, photo-electrochemical etching, Ideality Factor, Schottky barrier

1. Introduction

To reduce materials to nano-size and/or nano-thickness, most technologies are employed, resulting in novel and unique properties for materials in optical, electrical, optoelectronic, dielectric, etc. The result is the emergence of a brand new field of study known as thin films or coatings in the field of science. thin film is a thin film, the thickness of which ranges between several nanometers and just

a few micrometers [8], depending on the use. Metal-semiconductor Schottky contacts are important from a technological standpoint, therefore understanding their current–voltage (I–V) properties in depth is important [2]. With its superior characteristics and compatibility with silicon based electronics, metal-semiconductor junctions find several uses in microelectronic devices [3]. This area of research looks very promising. Metal-semiconductor interface states and chemical processes play a significant effect in device electrical characteristics [14]. The non-uniformity of interfacial charges is one factor that can lead to barrier inhomogeneity [7]. When compared to the current transport in a p-n junction, a metal/semiconductor junction is primarily owing to majority carriers, i.e. electrons for n-type semiconductors or holes for p-type semiconductors, The dominant process contributing to the metal/semiconductor junction current is the emission of thermally excited holes (or electrons) from a semiconductor to a metal over the potential barrier (thermionic emission, TE)

The PS layer is frequently placed between a c-Si substrate and a metallic contact layer [15]. Between the metal and the PS, a Schottky barrier is supposed to form, causing the PS layer to behave like a wide band gap semiconductor [6, 4]. Crystalline silicon metal/B-Si/c-Si is the most commonly studied device structure using PS layer. Crystalline silicon metal/PS/c-Si is the most commonly studied device structure that makes use of a PS layer. Metal/PS/c-Si/metal structures have identical rectifying qualities regardless of the metal chosen for the top contacts, according to studies on their electrical properties. As a result, device properties are determined by carrier transport inside the PS layer thickness and across the c-Si/PS hetero-junction. In order to make porous silicon photoconductors, oxidized porous silicon is coated with an aluminum film and then deposited on top of the aluminum film. The external quantum efficiency of porous silicon photodiodes could be improved by oxidizing the surface to make it passivated [1, 5, 13].

2. MATERIALS AND APPROACHES

Black silicon layers have made through electrochemical etching (ECE) and photo-electrochemical etching (PECE) on both p-type and n-type (100) silicon wafers. The substrate materials p and n-type silicon have a similar magnitude of resistivity (2 Ω.cm) and (5.50µm) thickness.

The wafers were cut into (1.5x1.5) cm^2 samples. The etching solutions is formed of HF (Hydrofluoric acid) and C_2H_5OH (Ethyl Alcohol) at concentration of (1:1). Samples were subjected to external illumination (Tungsten Lamp of 150 W). Silicon substrates were cleaned by using detergent with water, and then they were rinsed by ultrasonic bath filled with distilled water for 15 minutes. After that the substrates were rinsed by ultrasonic bath filled with pure alcohol for 15 minutes. Finally, the slides were dried by air blower and wiped with soft paper. Electrodes were thermally deposited using aluminum mask of 0.25mm thickness by thermal evaporation techniques at 10^{-5} torr pressure (Edwards coating unit system type E306A)for

deposition the Al and Ag electrodes on the etched silicon substrate. Diode layers is illustrated in fig. 1 (a ,b and c), the black circles are contact points.

forward and reverse biasing for I-V Characteristics test was carried out with (SOLAR CELL I-V TRACER IV26) device.

3. RESULTS AND DISCUSSION

I–V characteristics in dark for the black silicon /C-Si hetero-junction at various etching currents densities:

Figs. 2 and 3 show the forward and reverse biasing (I–V) characteristics of the n-Si and p-Si based devices respectively. At different etching current densities, and 25 min etching time. The linear characteristic allows determining the relevant diode parameters (ideality factor n).
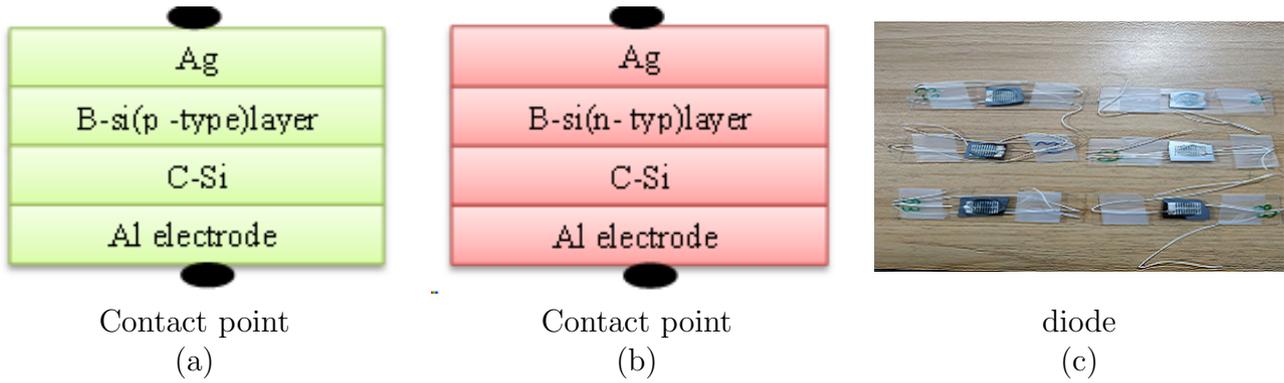
Contact point | Contact point | diode
(a) | (b) | (c)

Figure 1: cross-section view of the diode structure. (a) Ag/B-Si/p-Si/Al (b) Ag/BSi/ n -si/Al sandwich structure, (c) the diode

When the device is operated with a forward bias (at low voltages), the current increases exponentially as the depletion layer width decreases at the B-Si/c-Si interface. At the same voltage, reverse current is slightly increased with the applied voltage, causing electron-hole pairs to be created at low bias in all cases of reverse bias (for zero applied voltage exactly balances the diffusion current). A depletion layer expands in width, and the current is created by the voltage-dependent minority P-Si carriers. Minority carriers are dispersed through the link, which causes a current to flow. As junction structure improves, the number of defects at the junction's B-Si/c-Si contacts diminishes, and this leads to an improvement in reverse current flow. Crystal structural strain is responsible for these flaws.

The effect of the etching current density value on the diode current values is obvious in fig. 2 and 3. As these devices are operated under the similar external biasing voltage, the current values of the samples exhibit higher values related to the higher etching current densities [11].the I-V characteristics shows an increase in the forward current as the current density increase. This can be attribute to the different interfaces formed between pours silicon and bulk silicon (nano pours silicon) this leads to differences in the forward resistances of the prepared samples, although low values low of these resistances [10]
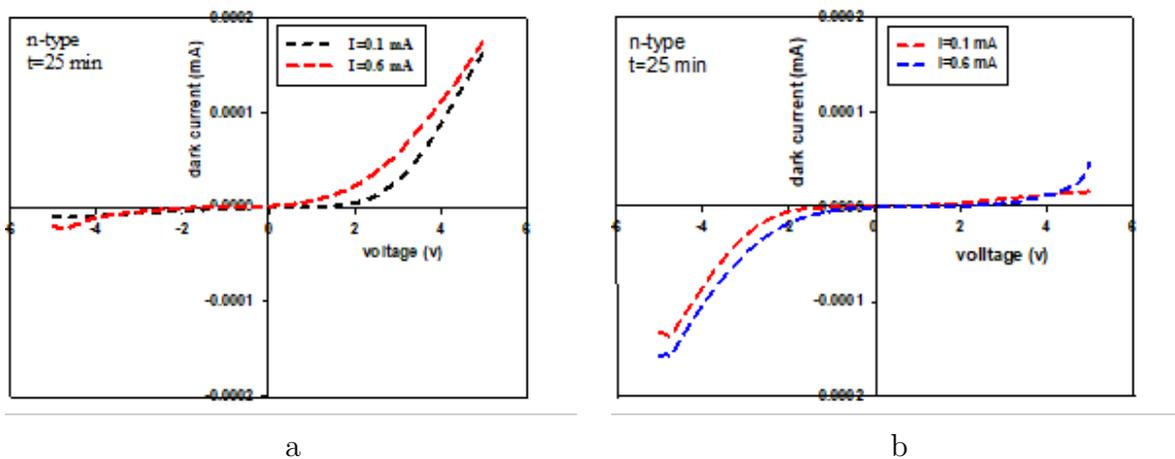

a | b

Figure 2: I-V characteristics of Al/B-Si/n-Si/Ag (a) Forward bias (b) Reversed bias

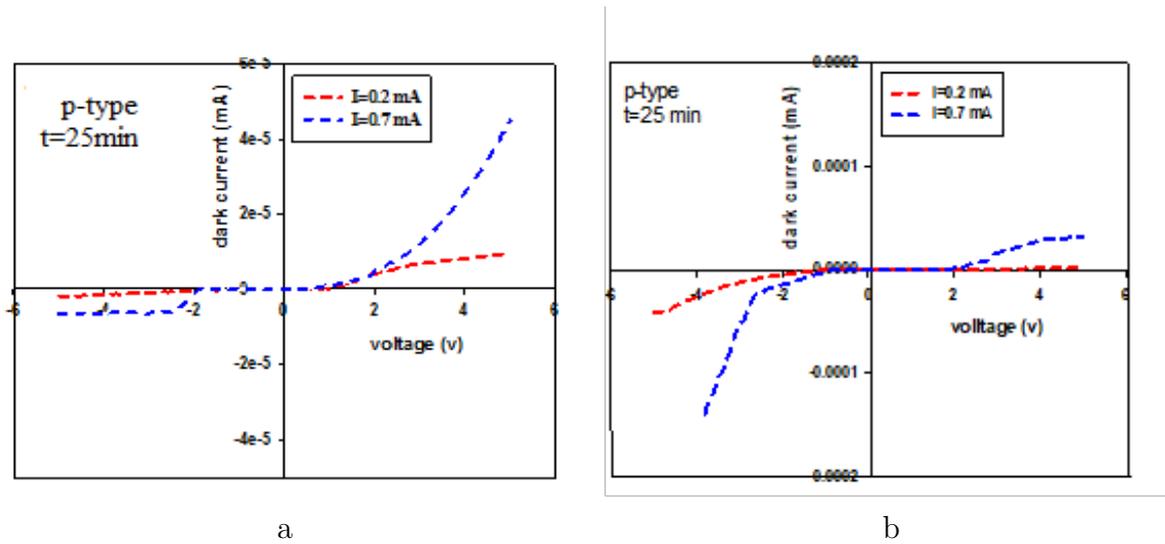a   b

Figure 3: I-V characteristics of Al/B-Si/p-Si/Ag, (a) Forward bias, (b) Reversed bias

4. Barrier height calculation

The barrier height is usually estimated using an extrapolation of the log(I) versus (V) curve to get the saturation current. the barrier height ($\emptyset B$) is computed from eq. (4.1). A diode saturation current is based on Schottky barrier height, according to a thermionic emission theory [12] by the following eq.:

$$\emptyset B = \frac{KT}{q}\ln(\frac{AA^*T^2}{I_s}) \tag{4.1}$$

Where I_s is the saturation current, K is the Boltzmann's constant, T is the absolute temperature, Φ_B is the barrier height, A is the surface area of the schottky diode and A^* is the effective Richardson coefficient which is equal to 32 and 112 for p-type and n-type silicon, respectively.

The barrier heights for Ag/B-Si/p-Si/Al and Ag/B-Si/n-Si/Al are listed in table 1 . As can be seen from Table 1, The current density (Js) of n-type Ag/B-Si/n-Si/Al increases and the barrier height decreases as the etching current increases (from 0.1 mA to 0.6 mA).

While in p-type, It was observed that the current density (Js) of p-type Ag/B-Si/p-Si/Al decreases and the barrier height increases as the etching current increases (from 0.2 mA to 0.7 mA).

This can be explained by the fact that the etching current density and time are not proportional to the BSi layer and BS/c-Si interface thickness. Depletion layer reduction at Ag/B-Si/n-Si/Al interfaces, combined with PS acting as series resistance, results in practically linear current-voltage characteristics (at higher voltages), and carriers can cross the potential barrier much more easily in the forward bias than in the low voltage bias, resulting in a reduction in the height of the potential barrier and an increase in diffusion current.

Inhomogeneity behavior at interfaces and on the metal-semiconductor boundary can be seen in the Schottky barrier height data, which demonstrate trap states exist. It is likely that the value of the barrier height depends on the interface atomic structure and atomic inhomogeneity at the metal-semiconductor interface generated by grain boundaries, multiple phases, facets and defects, in addition to the contact materials [12].

5. Ideality factor

A high ideality factor is due to a summation of ideal factors for each individual rectifying junction (i.e., Schottky diodes at the Ag/B-Si besides the two metal-semiconductor junctions (Ag/B-Si/c-Si/Al) of a diode perfectly have Ohmic characteristics). The ideally factor is calculated using equation (5.3) Table 1 summarizes the results. The ideality factor calculated from a slope of linear part of the forward bias (d ln I-V) characteristic via the relation in Eq. (5.3), as shown in Figs. (4 to 7 b). For practical diodes, the ideality factor is generally larger than unit [9]. The Schottky barrier height can be determined by using I-V curves as shown as in table 1. For thermionic emission and V>3KT, the general diode equations are in below:

$$I = Is \ \exp\{qv/(nKT)\} \tag{5.1}$$

$$Is = A^*AT^2 \exp\{-q\Phi_B/(KT)\} \tag{5.2}$$

$$n = \frac{q}{KT}(\frac{\partial V}{\partial In\ I}) \tag{5.3}$$

As can be seen for Table 1, The current density (Is) of n-type Ag/B-Si/p-Si/Al increases and the Ideality factor n decreases as the etching current increases for 0.1 mA to 0.6 mA respectively.
While, in p-type B-Si, it was observed that the current density (Is) of p-type Ag/B-Si/p-Si/Al decreases and the Ideality factor n increases as the etching current increases for 0.2 mA to 0.7 mA respectively.
The high lattice mismatch of B-Si and c-Si causes all values of ideality factor n to decrease with increasing etching current density, and the ideality factor n exhibits the identical behavior with cumulative etching time at constant current density. In other words, an inhomogeneous structure results in a large n ideality factor.
A density of trap states is very high. These traps are in charge for recombining the electron-hole pairs created as a result of the relatively high biasing voltage [9, 16].

Table 1: The saturation current density, the ideality factor and the barrier height of (Ag/B-Si/c-Si/A1) obtained from (I-V) characteristic curve.

Samples type	Is (mA/ cm^2)	Ideality factor(n)	Barrier height (ϕ_b) eV
0.1mA n-type Ag	6.86	36.63	0.3692
0.6 mA n-type Ag	6.95	27.47	0.3688
0.2 mA p- type Ag	7.73	28.28	0.3335
0.7 mA P-type Ag	7.05	35.61	0.3359

Other points reveal that the forward current decreases as the etching time rises, the explanation is as the etching time increases, the porous layer and porosity increase, causing the pore walls to act as carrier traps and create high resistance. However, such recombination currents do not flow uniformly throughout the structure, but rather at localized locations, such as extended flaws, etching time is affected by crystalline size and strain.
Many reports have been published at this time attempting to explain the mechanism governing the existing transport process using B-Si structures. The difference in junction area and Schottky barrier height of the dominant junction (Ag/B-Si, PS/p-Si, and p-Si/Al) for p-type and (Ag/B-Si, PS/n-Si, and n-Si/Al) for n-type is responsible for the rectifying behavior [16].

When draw Log Jf withe voltage volt can obtain curve as show as in fig.(4,5,6 ,7 a), when the circuit contact after applied electric field on the diode . the magnitude of current through the behavior is change according to voltage applied therefore the magnitude of current exploration to increase when the applied voltage the forward, the value of voltage applied the magnitude of voltage barrier is decreased while the current is under saturation because the applied effect resistance .

The slope of the linear part of the forward biasing (d ln I-V) .The ideality factor n determined from the slope of the linear region of the forward bias $(\partial V/(\partial \ln I))$ characteristic through the relation in Eq. (5.2),(5.3) which calculated from J_s and ln (J_f /J_s) as a function of bias voltage (V) as shown in Figs.(4,5,6 ,7 a)
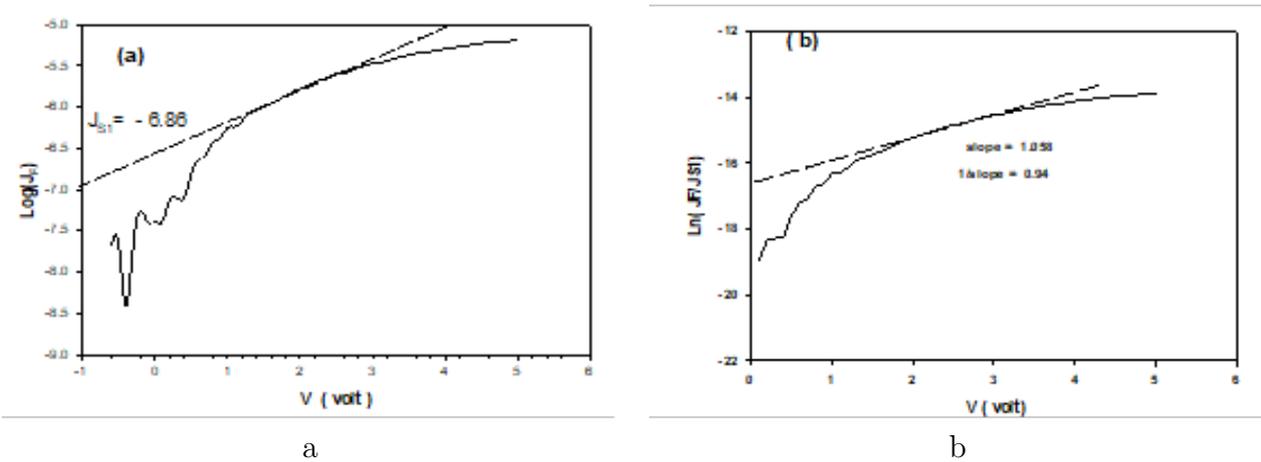

Figure 4: (a) log(J_F) (b) describe the relation between ln Jf/Js and voltage as a function of volt for forward bias applied to (0.1 mA) Ag/B-Si/n-Si/Al structures.
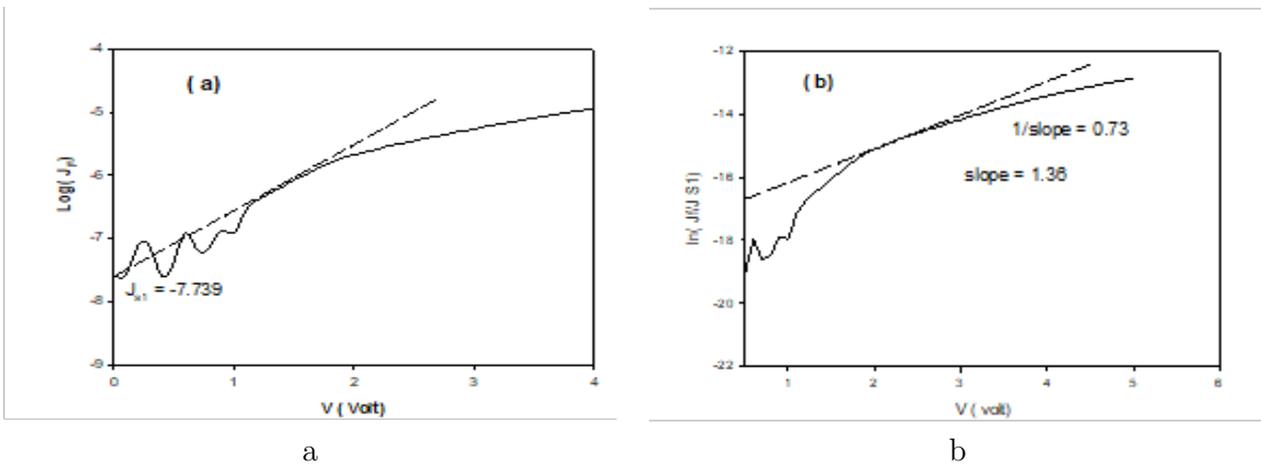

Figure 5: (a) log(J_F) (b)ln(J_F/Js) as a function of V for forward bias applied to (0.6 mA) Ag/B-Si/n-Si/Al structures.

6. CONCLUSION

In this work, we used B-Si structure to fabricate Schottky diodes for both p and n type silicon wafers. The main electrical properties , the I-V characteristics in dark nonlinear behavior under the forward biasing condition (at low voltages) it exhibits an exponential behavior with values increasing as the
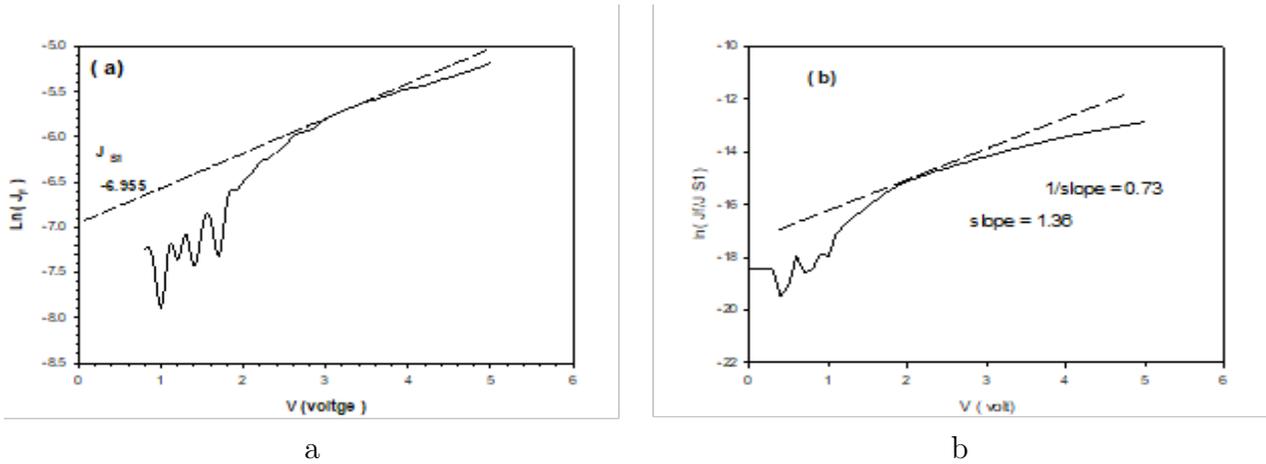
Figure 6: (a) $\log(J_F)$ and (b) $\ln(J_F/Js)$ as a function of bias voltage (V) at (0.2 mA etching current density sample of Ag/BSi/p-Si/Al diode structures.
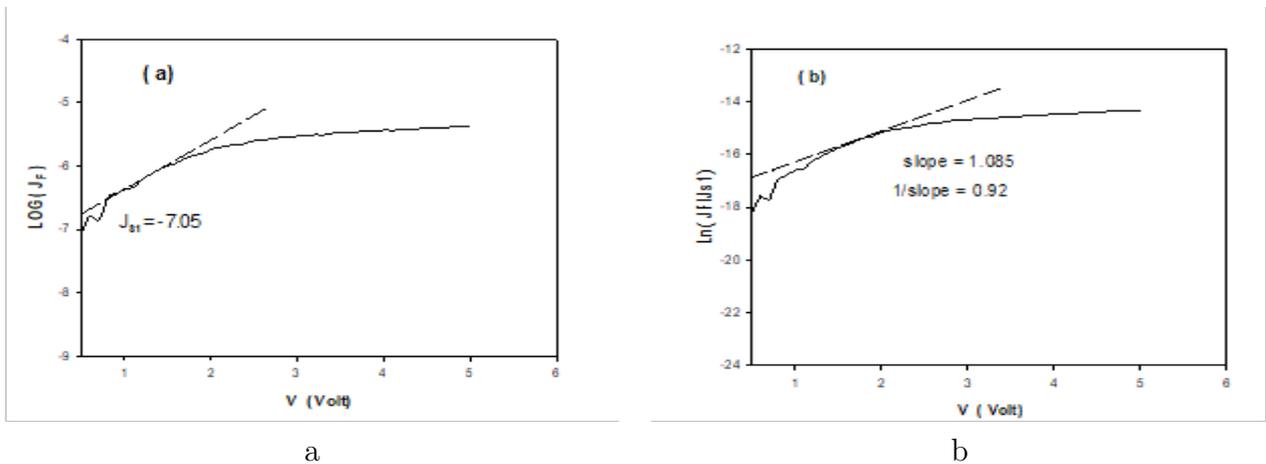

Figure 7: (a) $\log(J_F)$, (b) $\ln(J_F/Js)$ as a function of volt for forward bias applied to (0.7 mA) Ag/B-Si/p-Si/Al structures.

current increases. The consequences explain that the ideality factors for junctions signifying that this sample can offer a noble Schottky behavior. According to Schottky theory, the barrier height (ϕb) is completely determined by the metal's work function (Φm). When The saturation current density increases the ideality factors decrease in Ag/B-Si/n-Si/Al structure while The saturation current density decrease the ideality factors increases in Ag/B-Si/p-Si/Al structures .

Acknowledgments

References

[1] L. T. Canham, *Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers*, Appl. Phys. Lett. , 57 (1990) 1046-1048.

[2] Ö. Demircioglua, S. Karatas, N. Yıldırım, Ö. F. Bakkaloglu and A. Türüt, *Temperature dependent current–voltage and capacitance–voltage characteristics of chromium Schottky contacts formed by electrodeposition technique on n-type Si*, J. Alloys Compd. , 509(22) (2011) 6433-6439.

[3]   . R. S. Dubey, *Electrochemical fabrication of porous silicon structures for solar cells*, Nanosci. Nanoeng. , 1 (2013) 36-40.

[4]   H.A. Hadi, *Fabrication and characterization of Sn/PS/p-Si photodetector*, J. Coll. Educ. -Al Mustanseriyah Uni. –Baghdad–Iraq, 3 (2013) 634-647.

[5]   H. A. Hadi, *Comparative study of Schottky barrier heights of the different metals based onporous silicon prepared by photo-electrochemical etching (PECE)*, Mater. Focus. 3(6) (2014) 438-443.

[6]   H. A. Hadi, *Fabrication and electrical properties of FTO Nano-particles/Nanocrystal poroussilicon heterojunction under gamma radiation effect*,Mater. Sci.: An Indian J., 12(3) (2015) 100-106.

[7]   H. Li, D. He, Q. Zhou, P. Mao, J. Cao, L. Ding and J. Wang, *Temperature-dependent Schottky barrier in high-performance organic solar cells*, Sci. Rep., 7(1)(2017) 1-10.

[8]   A. Jilani, M. S. Abdel-wahab and A. H. Hammad, *Advance Deposition Techniques for Thin Film and Coating*, Modern Technologies for Creating the Thin-film Systems and Coatings (N. N. Nikitenkov, ed.), IntechOpen, 2017.`https://doi.org/10.5772/65702`.

[9]   U.M. Nayef, M. W. Muayada and H. A. Khalaf, *ZnO/PS/p-Si heterojunction properties*, Eur. Phys. J. Appl. Phys., 66(2) (2014), `https://doi.org/10.1051/epjap/2014130470`.

[10] M. Ohring, *The Materials Science of Thin Films*, Academic Press, , 1992, p. 137.

[11] Saymon, *Porous silicon formation by anodization*, Properties of porous silicon(L.T. Canham ed.) , Institution of Engineering and Technology, London, 1997, p. 176.

[12] . D. K. Schroder, *Semiconductor material and device characterization*, Third Edition, Arizona State University Tempe, Aza John Wiley & Sons, Inc, Publication, 2006, p. 192.

[13] R. Sharma, *Temperature dependence of I-V characteristics of Au/n-Si Schottky barrier diode*, J. Electron Devices, 8 (2010) 286-292.

[14] . Y. Sun, X. M. Shen, J. Wang, D. G. Zhao, G. Feng, Y. Fu, S. M. Zhang, Z. H. Zhang, Z. H. Feng, Y. X. Bai and H. Yang, *Thermal annealing behaviour of Ni/Au on n-GaN Schottky contacts* , J. Phys. D : Appl. Phys., 35(2002) 2648.

[15] S. M. Sze, K. K. Ng, *Physics of semiconductor devices*, 3rd Ed., John Wiley & Sons, Hoboken, New Jersey, 2006.

[16] D. F. Timokhov and F. P. Timokhov, *Determination of structure parameters of porous silicon by the photoelectric method.* J. Phys. Studies, 8(2), 173-177.