# Design and control strategy of solid state transformer using CHB, MMC and 5-L ANPC multilevel converters

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## Abstract

In this paper, the process of designing and comparing cascaded H-bridge (CHB) converter, modular multilevel converter (MMC), and five-level active neutral-point clamped (5L-ANPC) converter as a solid-state transformer (SST) utilized in the distribution network was investigated. The design was based on 1.7 kV IGBT modules (for CHB and MMC converters) and 3.3 and 4.5 kV IGBT modules (for 5L-ANPC converter). The converters were compared at voltage levels of 6.9, 11, and 20 kV and power levels of 0.5 and 2 MW. As well, when the number of MC voltage levels increases, the complexity of the control system, as well as the control algorithm, increases largely. In order to simplify the control system, a hierarchical control system is designed for these MCs. In the process of designing converters, thermal analysis and selecting smaller parts with lower losses due to enhanced efficiency were considered.

Keywords: Active NPC (ANPC), Cascaded H-bridge (CHB), Modular multilevel converter (MMC) efficiency, Modular multilevel converter (MMC), Solid state transformers (SST), Control systems
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## 1 Introduction

Electrical energy generation, transmission, and distribution are three major components of a power system, where transformers play a crucial role. A transformer is a major device that bridges generation and consumption [3]. As high power converters, SSTs are of great interest to researchers and have been widely investigated for use in electrical energy distribution systems [9, 12]. The solid state transformer ( SST ) was conceived as a replacement for the conventional power transformer, with both lower volume and weight [4]. Multilevel converters (MCs) are produced by connecting independent semiconductor devices in various configurations, and provide functioning at voltages and currents that exceed the nominal value of the devices. These MCs have advantages such as low common-mode voltage, low dv/dt stress, low electromagnetic interference (EMI) noise or interference, and enhanced efficiency. It is required control frequency of MC is extremely high, which makes the traditional centralized control system hard to cope with and seriously aggravates the algorithm burden of main control chip. Besides, as the number of cascaded sub-modules in

MMC is quite large, a large number of optical fibers are directly connected to the main controller in the traditional centralized control system, which makes the wiring difficult and decreases the system modularity. As a result, MCs are utilized in various applications, including grid-tied inverters, active front end (AFE) rectifiers, high-voltage direct currents (HVDCs), motor drives, and FACTS devices. MCs are classified into three general categories.

- Neutral-point clamped (NPC)

- Flying capacitor converter (FLC)

- Cascade converters

The cascade topology is divided into two categories: Cascaded H-Bridge (CHB) and Modular Multilevel Converter (MMC). Various types of MCs are used in commercial applications for motor drives. One example is low voltage drives, such as two-level voltage source inverters and three-level NPCs. Today, multilevel converters are interesting high-power converters in industrial and academic areas. A multilevel converter can generate the desired voltage through a combination of step voltages. The most important advantage of multilevel converters lies in their application in low-voltage semiconductor devices. This reduces switching losses and voltage stress on power electronic components [10, 5, 8, 2]. Many studies compared multilevel converters. The CHB, MMC, and ANPC converters were compared to meet motor drive requirements [1]. The components were measured, and the converters were compared in efficiency. Also, the designed LC filters were compared in the output stage. ANPC, CHB, and MMC converters were designed and compared at three voltage and power levels [13, 6, 11]. CHB and 5L-ANPC converters have been used for medium voltage drives (operating at 4 to 6.9 kV) by ABB in the product ACS2000. This topology has been obtained by modifying the three-level NPC structure and adding a cell to its output. The 5L-ANPC topology has been designed based on medium-voltage semiconductors and, compared to traditional NPCs, employs fewer semiconductors and capacitors. Finally, the MMC topology has been used in drive motors up to 4 MV. In this paper, CHB, MMC, and 5L-ANPC converters were compared at voltage levels of 6.9, 11, and 20 kV and power levels of 0.5 and 2 MW. Converters were considered SSTs to rectify and convert three-phase source voltage levels to DC voltage for transmission. DC transmission paths, known as HVDCs, are slowly increasing in power transmission networks using power electronic devices and converters. At the end of the path, there exists a DC to AC converter to convert DC voltage to usable voltage for a three-phase load.

In the design of the topology of electronic power converters, thermal analysis and choosing smaller parts with fewer losses are of paramount importance due to enhanced efficiency. Table 1 summarizes common specifications in all three CHB, MMC, and 5L-ANPC converters for different simulation modes. In Table. 1, the specifications that are identical for different simulation moods are presented.

Table 1: Common specifications in different simulation moods

| Specification | Features |
|---|---|
| Three-phase input source specifications | 6.9, 11 or 20 kV with star-delta connection and a frequency of 50 Hz |
| DC transmission path specifications | A hypothetical length of 1 km, RC branch (0.1 m $\Omega$ and 0.3 $\mu F$) and RL branch (0.2 $\Omega$ and 0.5 H), inductive and capacitive properties in transient state |
| Output inverter specifications (DC to AC conversion) | Inverter has three IGBT/Diode-based arms, converting to the voltage level of 20 kV and a frequency of 50 Hz |
| Specifications of the RL filter in the inverter output to eliminate current spikes caused by switching | Inductance of 1 mH and a resistance of 10 m $\Omega$ |
| Load specifications | 20 kV, three-phase, star-delta connection with a frequency of 50 Hz |
| Switching frequency of converters | 3 kHz |
| Sample time of simulation implementation | 10 $\mu s$ |
| Final output DC link voltage of converters (transmission path) | 1050 v (internal DC link of converters is not the same) |

## 2 Design and selection of parts

The first step in designing a converter is to select the DC link voltage level. The minimum DC voltage level demanded in the converters discussed in this report needs to be defined based on eliminating the sixth harmonic amplitude. Assuming that the voltage value should rise by 15% to eliminate the third harmonic amplitude, as follows:

$$V_{dc,CHB} = \frac{V_{L-L}}{\sqrt{2}} \tag{1}$$

$$V_{dc,MMC} = V_{dc,ANPC} = V_{L-L} \times \sqrt{2} \tag{2}$$

A proper percentage of reverse voltage must also be assumed to supply the minimum voltage required to ensure transducer operation in transient states. Typically, the reverse voltage is 10% of the DC link voltage. Table 2 presents the internal DC link voltage of the converters. This voltage is generated on the capacitor bank. The voltage levels of the internal dc link voltage are shown in Table 2.

Table 2: Internal DC link voltage levels in converters

| Converter/ Voltage | 6.9 kV | 11 kV | 20 kV |
|---|---|---|---|
| CHB | 5.4 | 8.6 | 15.6 |
| MMC | 10.7 | 17.1 | 31 |
| 5L-ANPC | 10.7 | 17.1 | 31 |

In designing these converters, it is attempted to utilize high voltage elements such as 1.7 kV IGBTs to mitigate losses and enhance efficiency.

## 3 Selection of passive circuit elements

Passive elements refer to capacitive filters and other elements that confine voltage and current spikes. The total voltage of the DC link and ripple and associated hopping should not transcend 70% of the capacity of IGBTs. Series IGBTs and voltage dividing are techniques to diminish voltage stress on IGBTs. Furthermore, when a rectifier diode class is demanded, the equivalent diode voltage must be determined from the equation below, where k is a reliability coefficient, typically 2 or 2.5.

$$V_{Blocking} = \sqrt{2} \times V_{Grid} \times k \tag{3}$$

The main advantage of utilizing electronic power converters as SSTs instead of traditional transformers is mitigating the level of harmonics by controls. The capacitance of DC link converters under various conditions is given in Table 3.

Table 3: The capacitance of DC link of converters in $\mu F$

| Converter/ Voltage | 6.9 kV | | 11 kV | | 20 kV | |
|---|---|---|---|---|---|---|
| CHB | 1250 | 2500 | 1250 | 2500 | 1250 | 2500 |
| MMC | 2000 | 2000 | 2000 | 2000 | 2000 | 2000 |
| 5L-ANPC | 2000 | 2000 | 2000 | 2000 | 2000 | 2000 |

The DC link voltage level is the main factor to consider in selecting a capacitor, as the capacitor is responsible for repulsing voltage ripples. The capacitor of all converters has been chosen for the highest voltage level in the simulation. Hence, a reliable and practical capacitor bank has been used at different voltage levels. This is because the conditions need to be the same for optimum comparison maximally.

For the CHB converter, the value of the DC link capacitor was considered different at various powers to enhance THD. This is because instantaneous and transient currents increase upon increasing power at the same voltage level. As the capacitor becomes larger, the currents are used to charge the DC capacitor, avoiding transient states and initial spikes.

## 4 Control of converters

This section deals with the process of controlling the converters.

## A) CHB converter

The best method to control a CHB converter is PWM or PSPWM modulation. Compared to other methods, this method produces less THD at the output and leads to fewer losses on the switches. In this method, it is not crucial to control the DC voltage of the diode. This section briefly describes the control scheme of a single phase, which is based on the cascade connection of three decoupled stages. This control scheme was developed in [6, 7, 11], and is depicted in Fig. 1. To achieve optimal performance, a control loop for the dq components of the estimation error is needed so that A and $\theta$ are correctly estimated. For this purpose, two independent proportional-integral (PI) controllers in the synchronous frame are proposed to process $\epsilon d$ and $\epsilon q$ in order to determine $\Delta A$ and $\Delta \theta$, respectively, as:

$$\Delta A = K_{pa}\epsilon_d + K_{ia} \int \epsilon_{ddt} \tag{4}$$

$$\Delta\theta = \frac{K_{pa}}{A0}\epsilon_d + \frac{k_{ia}}{A0} \int \epsilon_{ddt} \tag{5}$$

The parameters $k_{pa}$ and $k_{ia}$ are the proportional and integral gains of the PI controllers.
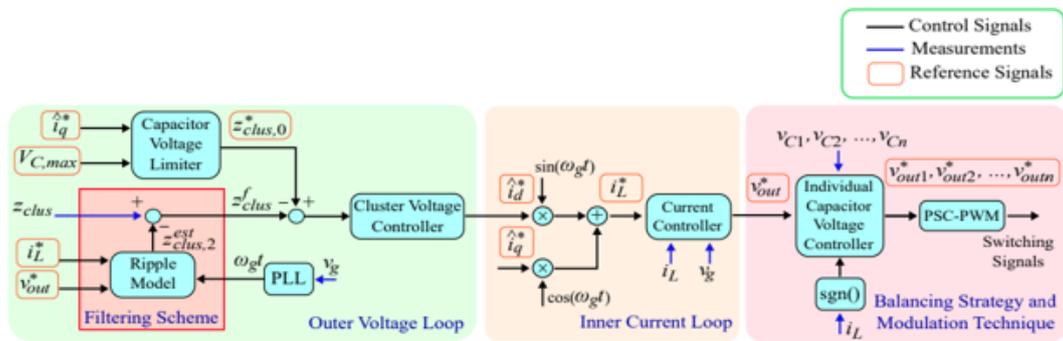


Figure 1: An overview of cascade control scheme

## B) MMC converter

In this converter, the Phase Shifted PWM or PSPWM method is utilized. This method produces smaller THD at the output, and thus fewer losses occur on the switches. Compared to the traditional centralized MMC control system [5, 8], the added valve control layer separated the whole control system into three layers as layers of main controller, valve controllers and unit controllers. Communication between different control layers is realized by high-speed fiber-optic serial communication. The proposed hierarchical control structure makes the control process distributed in different control layers and thus the algorithm burden of main controller is reduced. Algorithm division in different layers is listed as; 1) Main controller: As the core of the whole control system, main controller accepts instructions from control platform, executes MMC control algorithm, 2) Valve controller: A Valve controller integrate several UMs into a VM. As a medium control layer, valve controllers respond to both the upper and the bottom control layer. For the main controller, valve controllers accept instructions from it and feedback capacitor voltages and failure information. For the unit controllers, valve controllers communicate and get capacitor voltages and failure information of each UM inside it and then assign connected index to each UM by executing a certain capacitor voltage balancing method, 3) Unit controller: A unit controller accepts connected index from the valve controller, acquire capacitor voltage and feedback working state and capacitor voltage to valve controller.

## C) 5L-ANPC converter

In this report, the SPPWM method has also been used in the 5L-ANPC converter. Due to the layer structure, this method is applied to this converter as Level Shifted. Furthermore, other papers have also used methods such as Selective Harmonic Elimination (SHE) modulation. This proposed method can effectively reduce the number of switching states involved in the rolling optimization, so the efficiency of the processor will be improved. In addition, because of the difficulty at selecting weight factors in predictive control, the design method of weight factor in the SHE controller will be also described in previous study [11].

# 5  Modeling and simulation

The simulation file is demonstrated in Figure 1. In this simulation, the input is a three-phase source with a frequency of 50 Hz, having variable voltages of 6.9, 11, and 20 kV in different modes. The three-phase output enters the electronic power converter, which acts as an SST, and is converted to DC mode. The load or final consumer of the three phases is supposed to locate at the end of the distribution network. The network is DC and is supposed to have a length of 1 km. At the end of the distribution path, there is a DC to AC inverter converter. There is also an RL in the converter output to eliminate current distortion and enhance the load current quality. Table 1 summarizes the parameters of the simulation model. The power electronic converter, acting as an SST, is shown in green. The green block is substituted in different simulation modes by the CHB, MMC, or 5L-ANPC converter.

In traditional distribution networks, a typically large step-down transformer is utilized to alter the voltage level. An SST is employed to diminish the transformer dimensions and improve the harmonic effects and reactive power consumption. These transformers are power electronic converters intended to convert voltage and current levels. A traditional small transformer is also used in some types of these transformers.

An SST receives voltages in kV at the input and converts it to DC. On the user side, another SST converts DC voltage to AC with the required frequency and voltage.
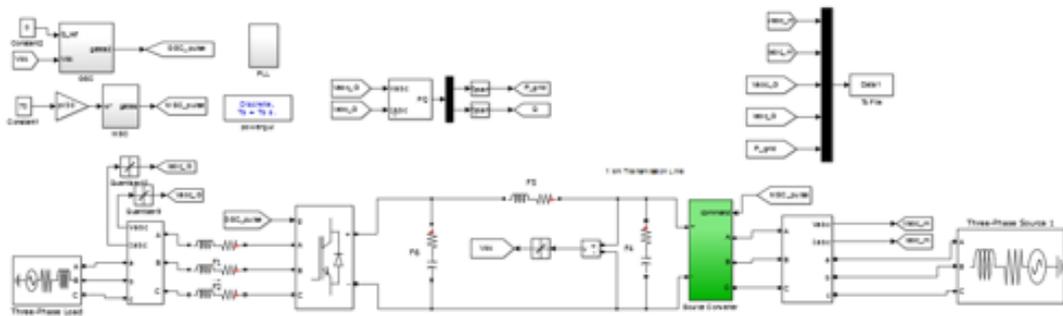


Figure 2: An overview of the simulated circuit

MSC and GSC blocks are used to control the converter on the source and user sides, respectively. The interior design of the MSC block is demonstrated in Figure 3. This controller consists of two internal and external loops. The inner loop controls the three-phase voltage (within the dq0 reference frame) based on the SVM method, where its output provides a PSPWM pulse for the converters. Generated by the PSPWM method, this pulse can be utilized for all CHB, MMC, and 5L-ANPC converters. Furthermore, to achieve an optimum comparison, it is suggested to use the same method for all converters. The external control loop depicted in Figure 3 acts to control the source current. All control loops use a PI controller.
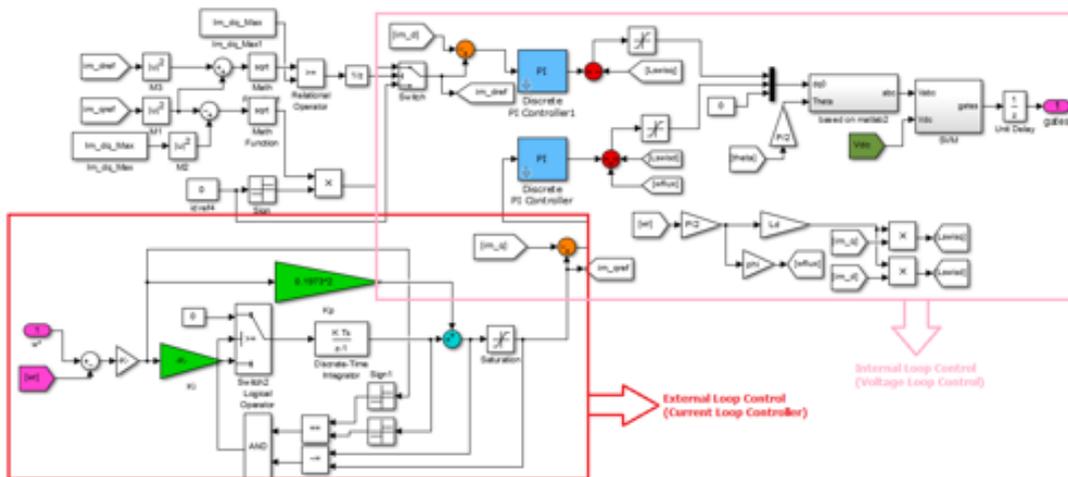


Figure 3: The interior design of the MSC block
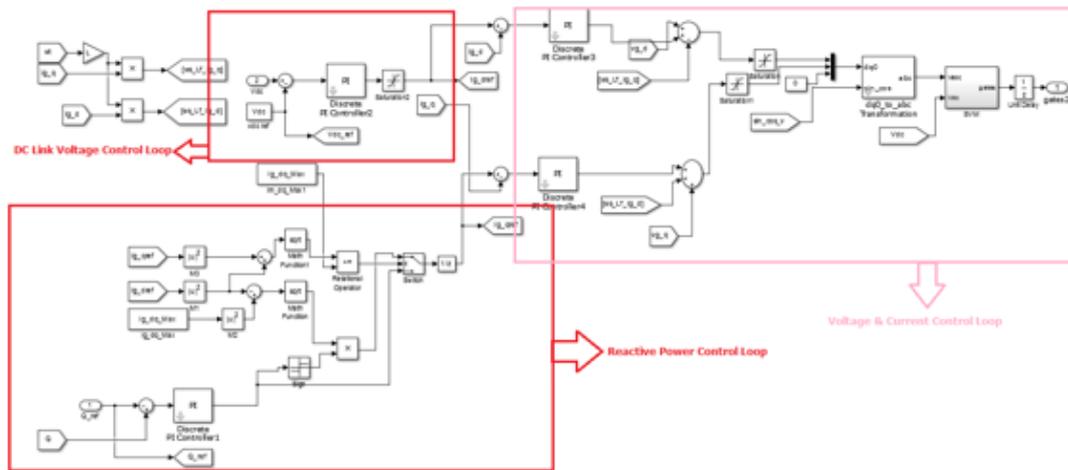
Figure 4: The interior design of the GSC block

Figure 4 demonstrates the interior design of the GSC block. This controller is made of two internal loops and two external loops. The inner loop serves to control the three-phase load voltage (within the dq0 reference frame) based on the SVM method. Its output provides the PSPWM pulse for the DC to AC inverter. The external control loop illustrated in Figure 3 controls the reactive load power consumption and the DC link voltage. All control loops utilize a PI controller. The block diagrams of CHB, MMC, and 5L-ANPC converters are depicted in Figures 5 to 6, respectively. The internal DC link voltage levels and the capacitance of the converters are summarized in Tables 2 and 3, respectively.
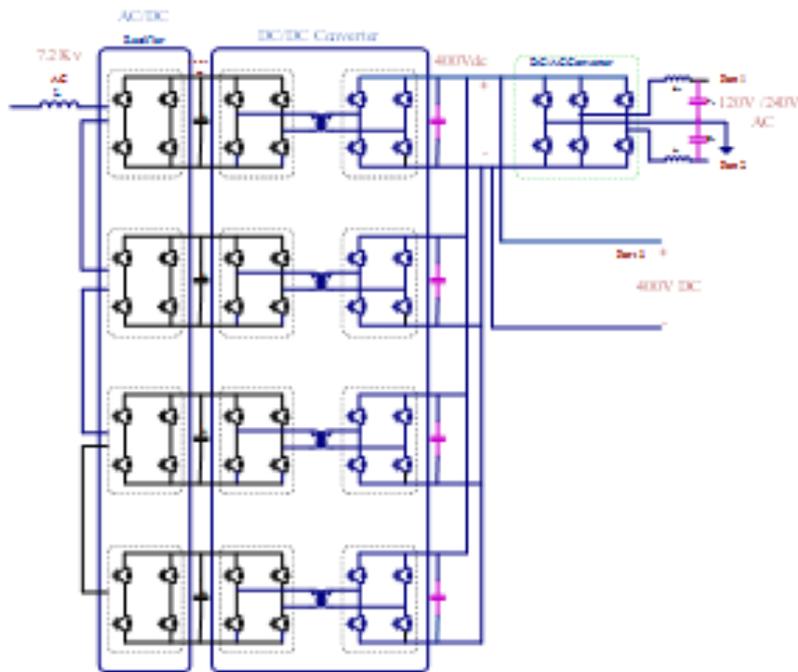


Figure 5: The block diagram of the CHB converter
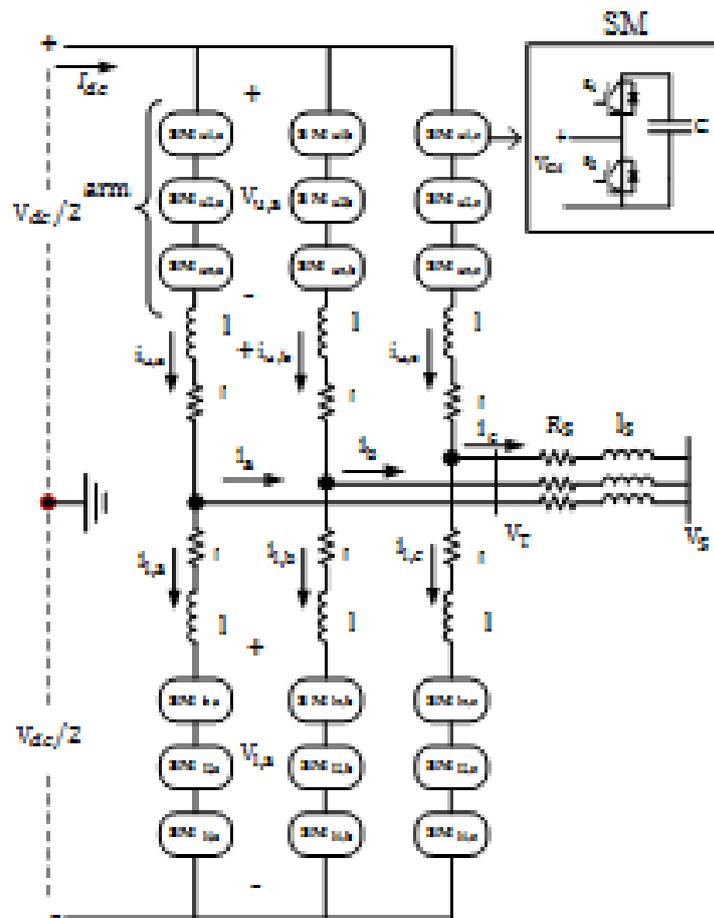
Figure 6: The block diagram of the MMC converter
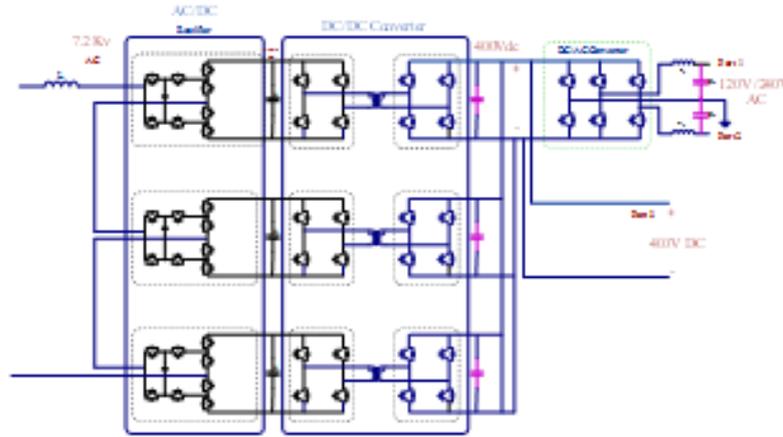
Figure 7: The block diagram of the 5L-ANPC converter

# 6 Simulation results and comparison tables

This section presents simulation results and comparison tables. The simulation results for the CHB converter at voltages of 6.9, 11, and 20 kV and capacities of 0.5 and 2 MW are shown in Figures 8 to 13. At the same voltage and power levels, the results for the MMC converter are shown in Figures 14 to 19, and that of the 5L-ANPC converter are demonstrated in Figures 20 to 25.

## 6.1 Cascade H-Bridge converter results

In this section, the voltage and current waveforms at the input and output sides are drawn for the CHB converter under various input voltage and power levels.
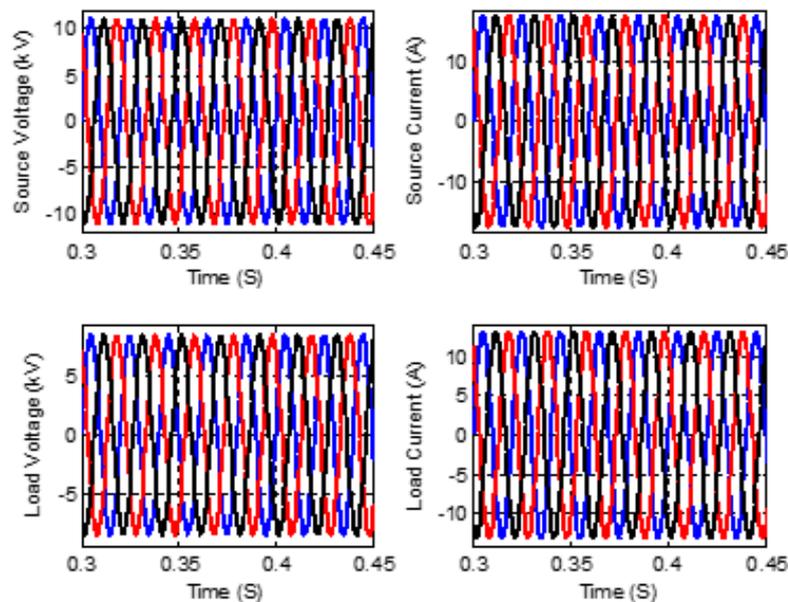


Figure 8: The waveform of voltage and current at the input side and CHB load for a voltage of 11 kV and a power of 2 MW

## 6.2 MMC converter results

In this section, the voltage and current waveforms at the input and output sides are drawn for the MMC converter under various input voltage and power levels.
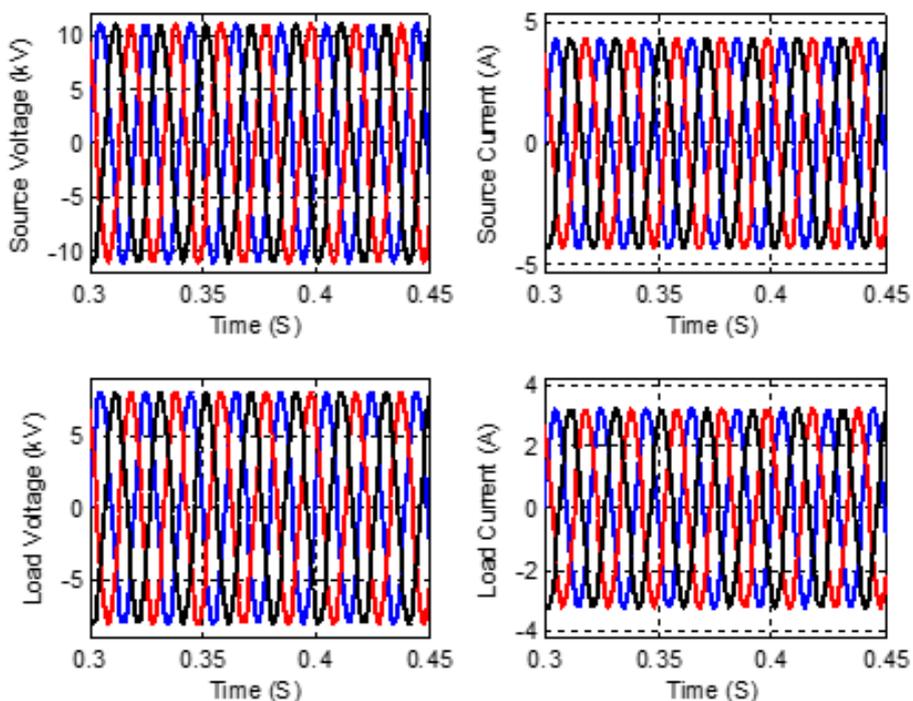
Figure 9: The waveform of voltage and current at the input side and CHB load for a voltage of 11 kV and a power of 0.5 MW
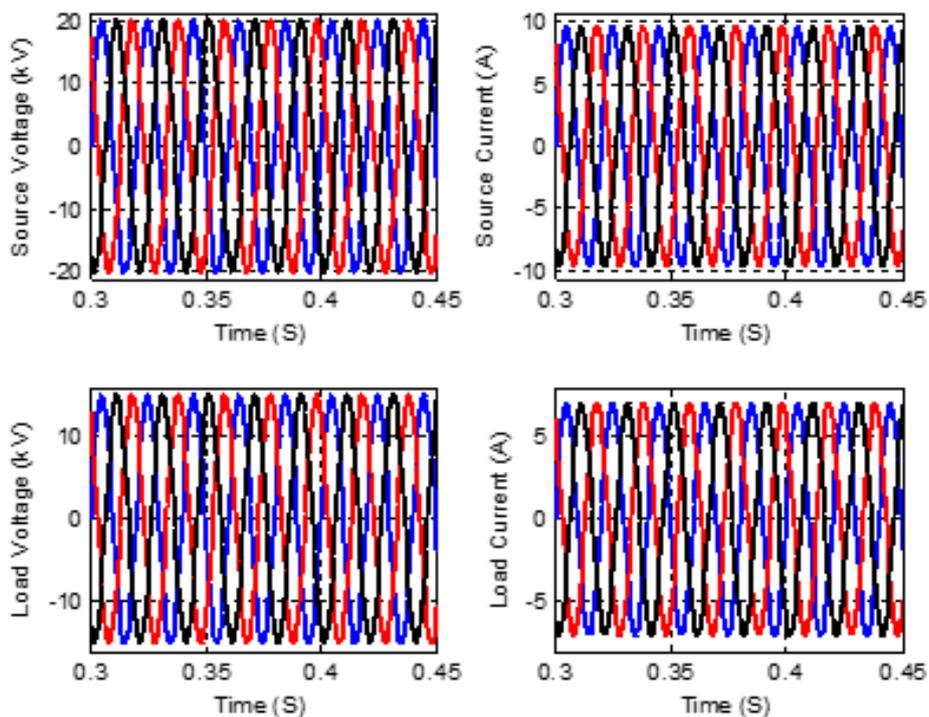


Figure 10: The waveform of voltage and current at the input side and CHB load for a voltage of 20 kV and a power of 2 MW

## 6.3 5L-ANPC converter results

In this section, the voltage and current waveforms at the input and output sides are drawn for the 5L-ANPC converter under various input voltage and power levels.
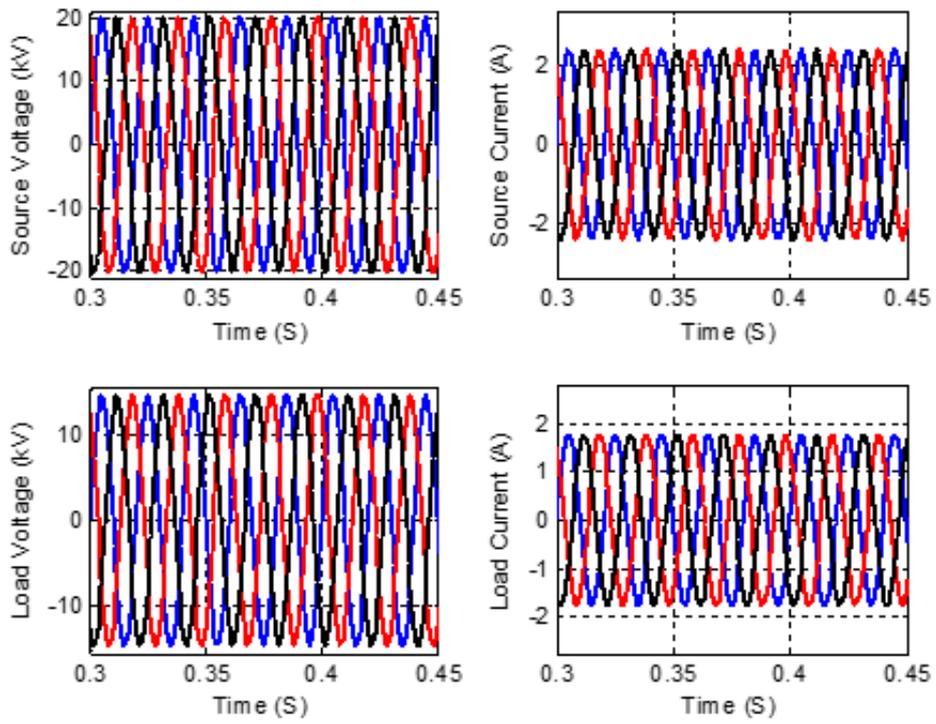
Figure 11: The waveform of voltage and current at the input side and CHB load for a voltage of 20 kV and a power of 0.5 MW
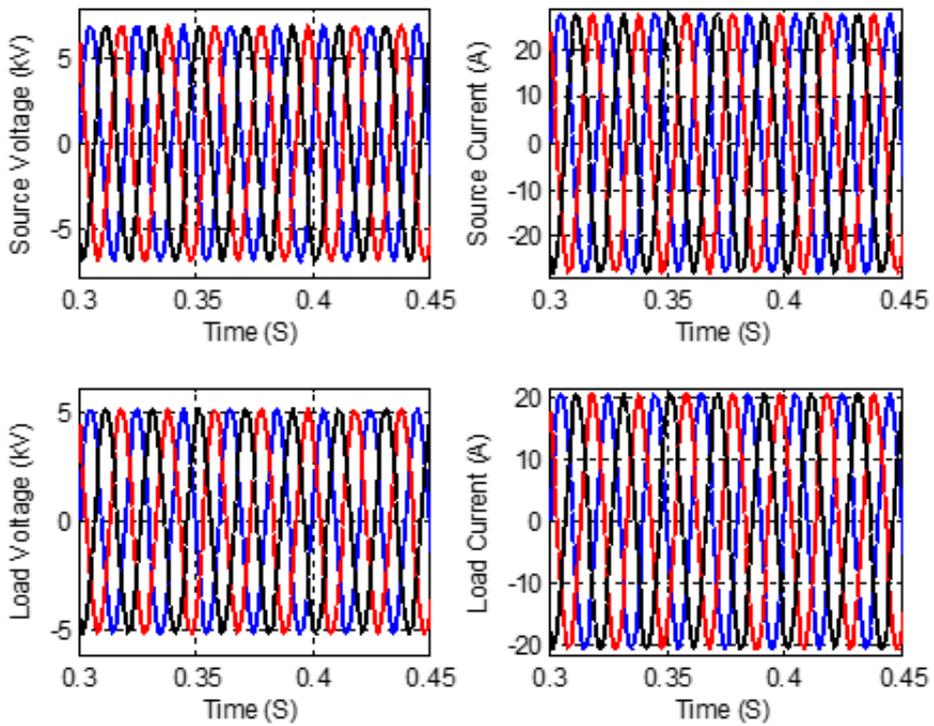


Figure 12: The waveform of voltage and current at the input side and CHB load for a voltage of 6.5 kV and a power of 2 MW
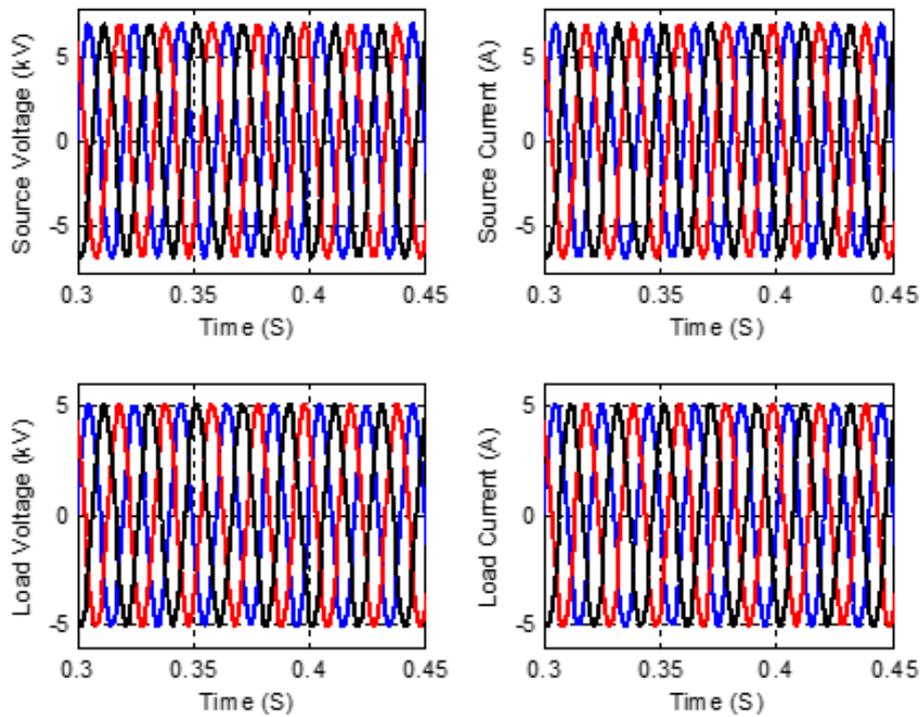
Figure 13: The waveform of voltage and current at the input side and CHB load for a voltage of 6.9 kV and a power of 0.5 MW
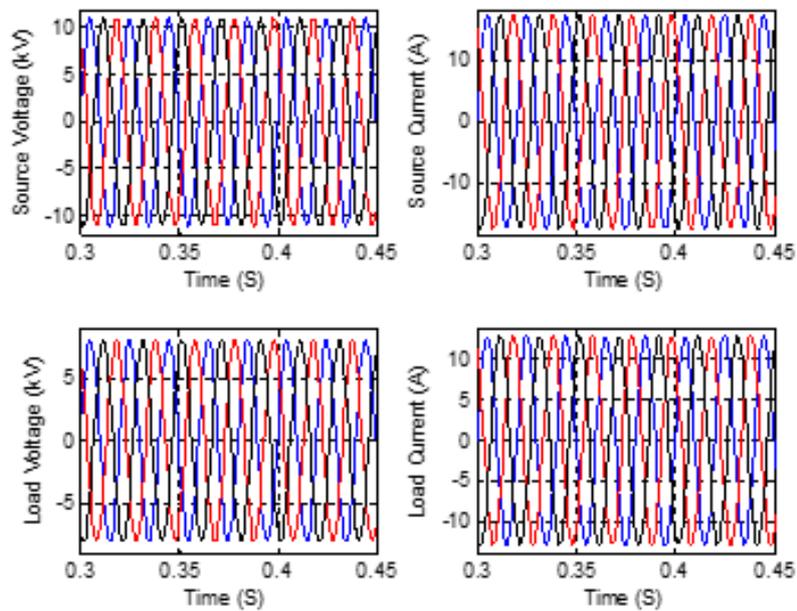


Figure 14: The waveform of voltage and current at the input side and MMC load for a voltage of 11 kV and a power of 2 MW
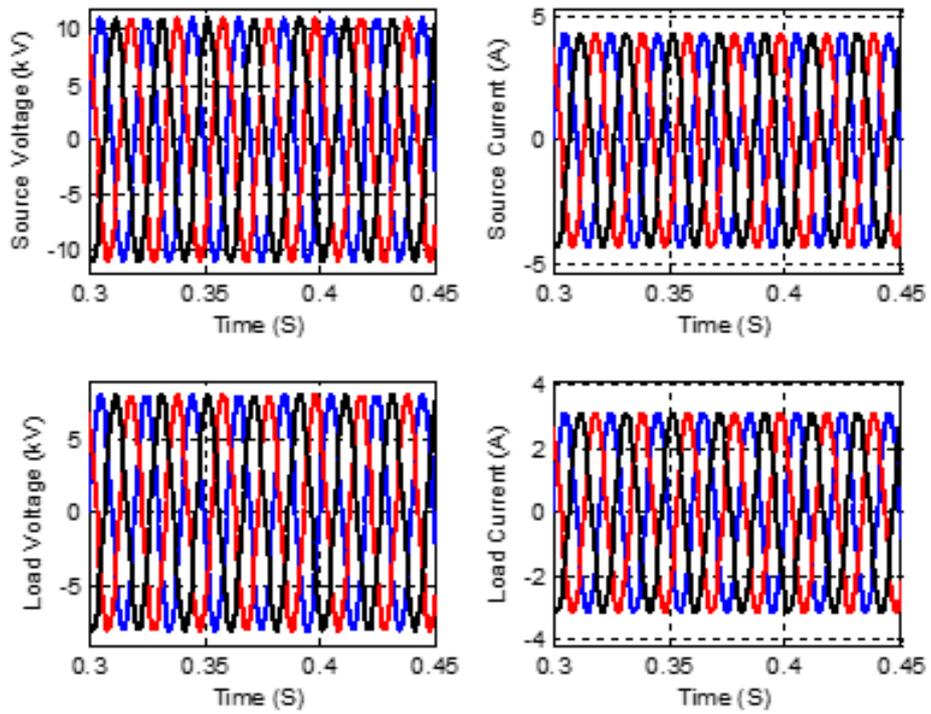
Figure 15: The waveform of voltage and current at the input side and MMC load for a voltage of 11 kV and a power of 0.5 MW
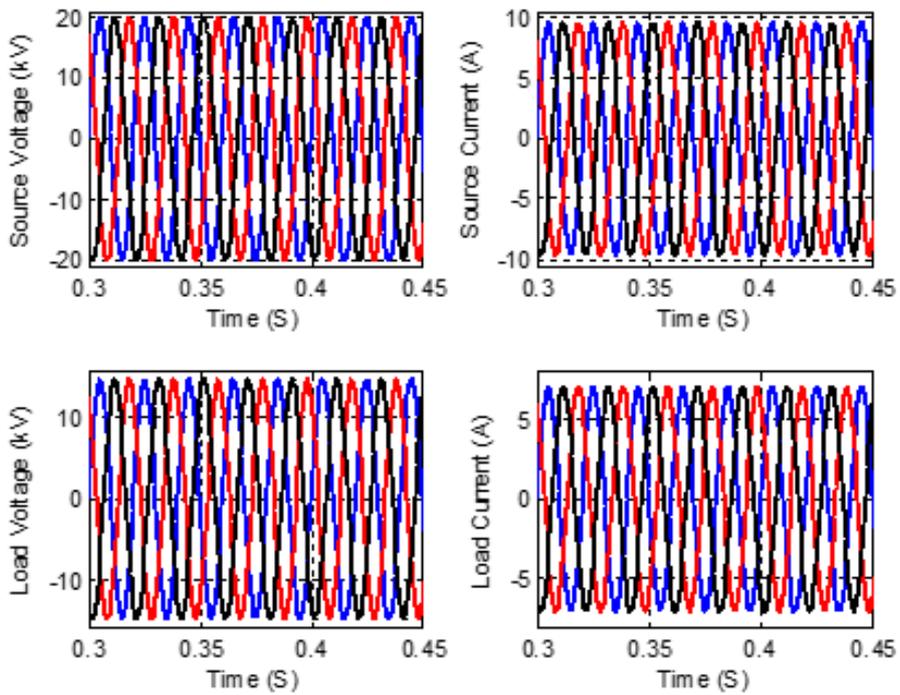


Figure 16: The waveform of voltage and current at the input side and MMC load for a voltage of 20 kV and a power of 2 MW
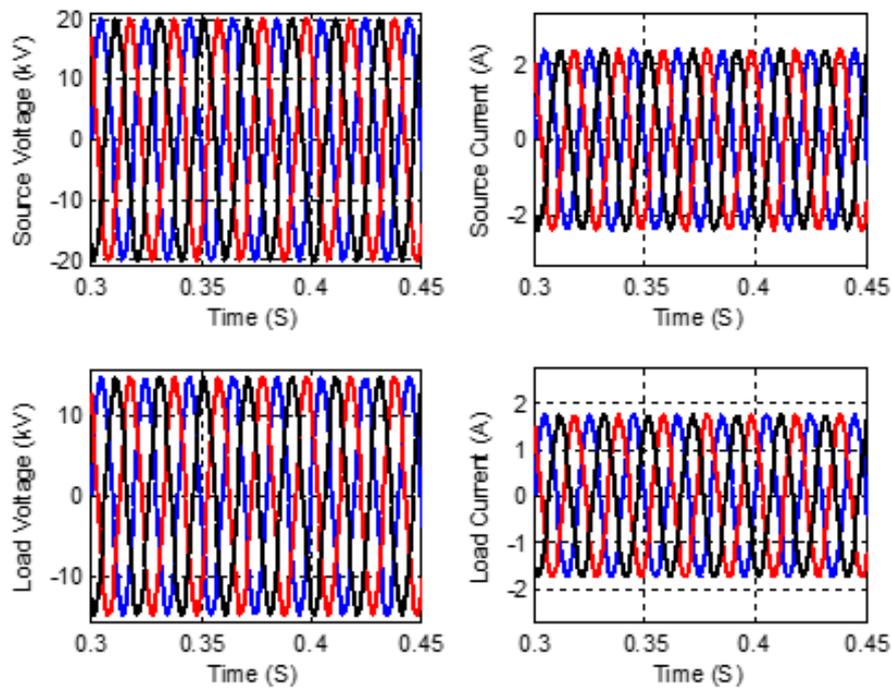
Figure 17: The waveform of voltage and current at the input side and MMC load for a voltage of 20 kV and a power of 0.5 MW
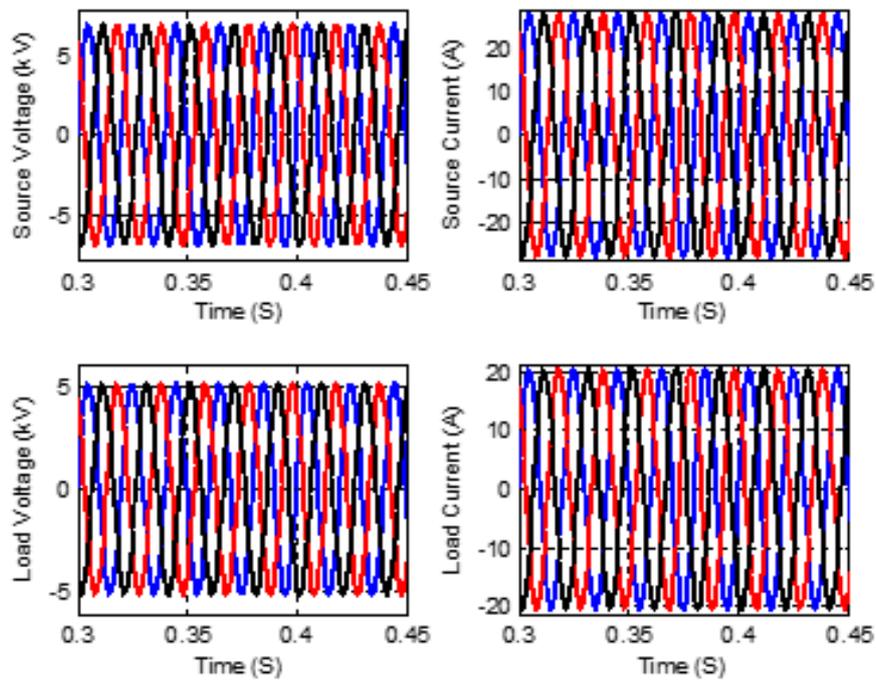


Figure 18: The waveform of voltage and current at the input side and MMC load for a voltage of 6.5 kV and a power of 2 MW
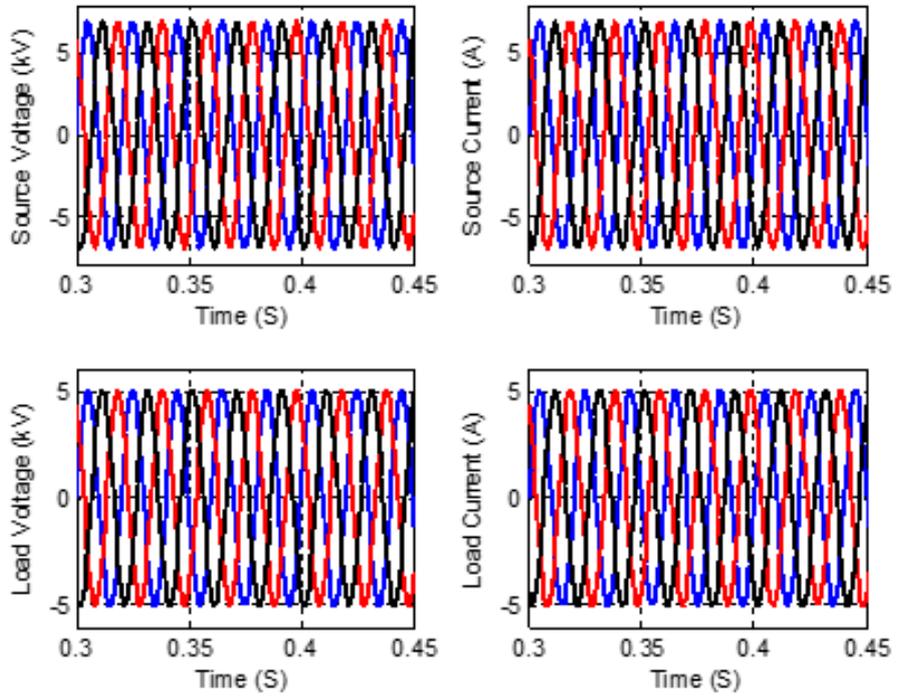
Figure 19: The waveform of voltage and current at the input side and MMC load for a voltage of 6.9 kV and a power of 0.5 MW
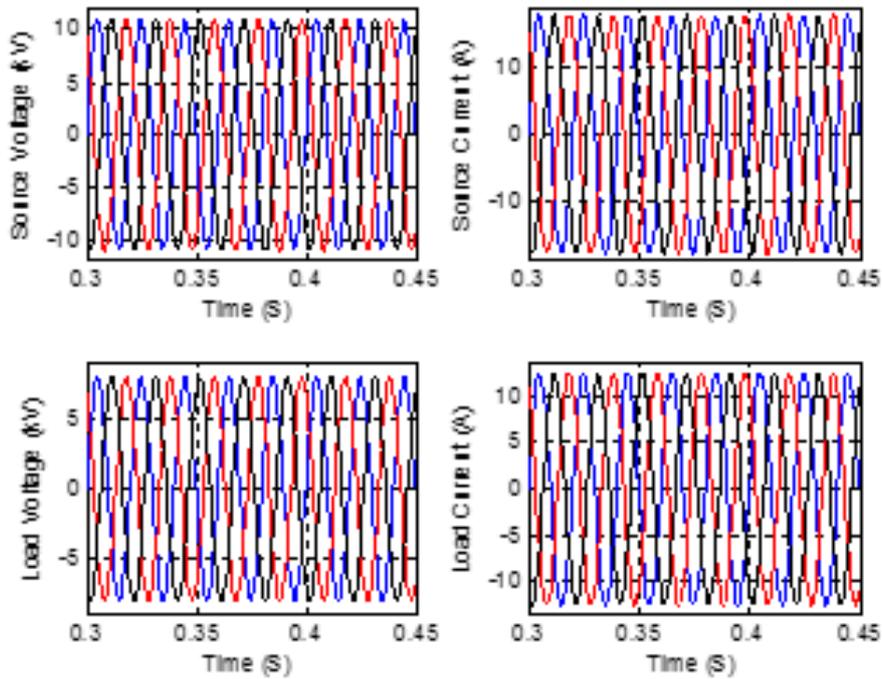


Figure 20: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 11 kV and a power of 2 MW
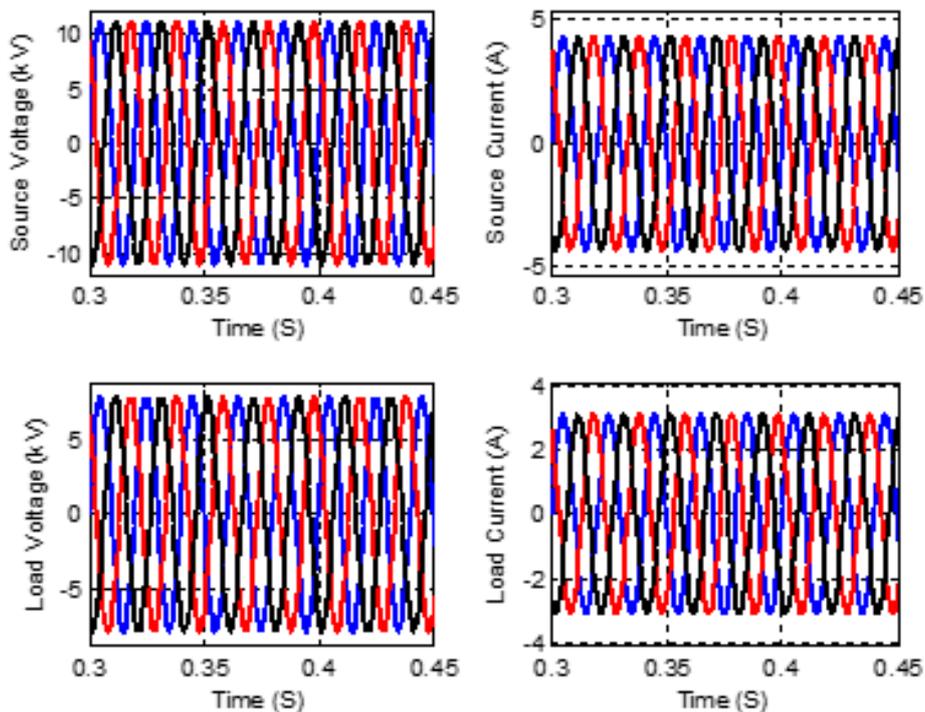
Figure 21: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 11 kV and a power of 0.5 MW
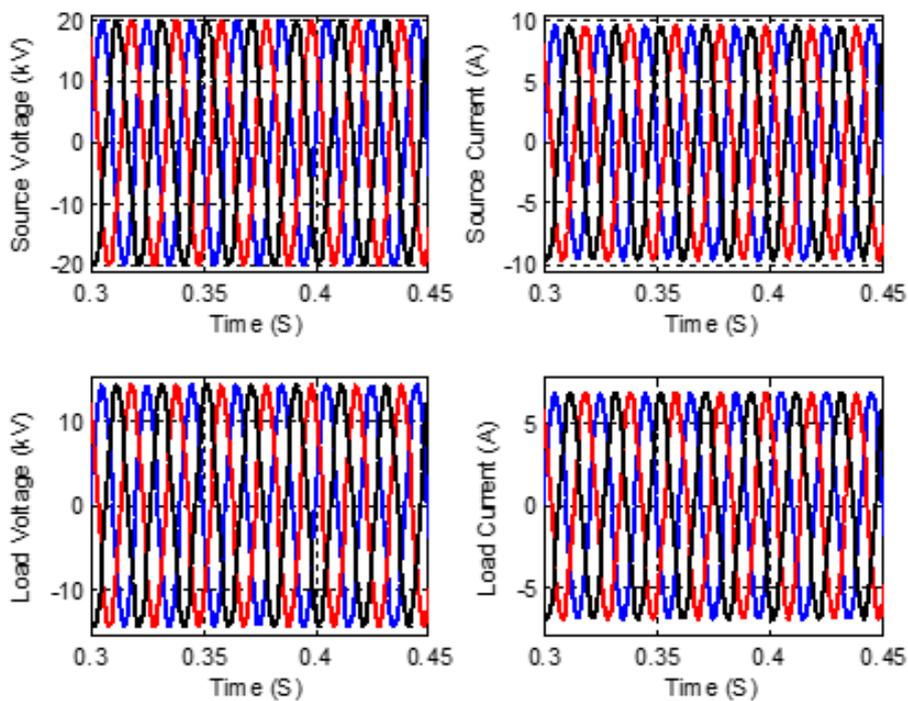


Figure 22: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 20 kV and a power of 2 MW

## 6.4 Discussion and comparison

In this section, converters are compared in terms of switch efficiencies, energy storage elements, the number of circuit elements, and the voltage and current of IGBTs. Table 4 compares the efficiency of converters under different
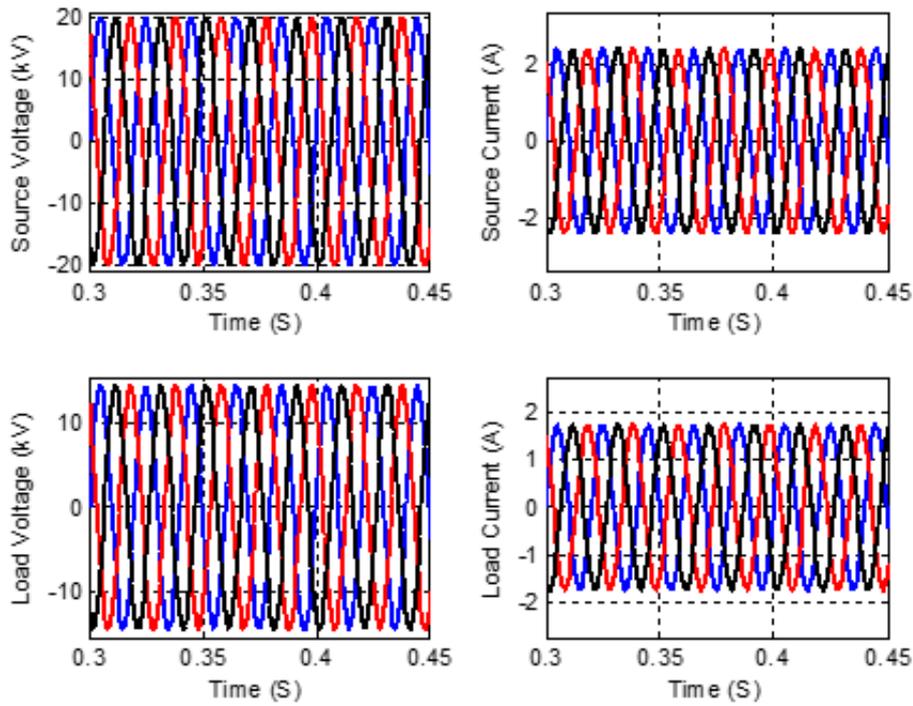
Figure 23: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 20 kV and a power of 0.5 MW
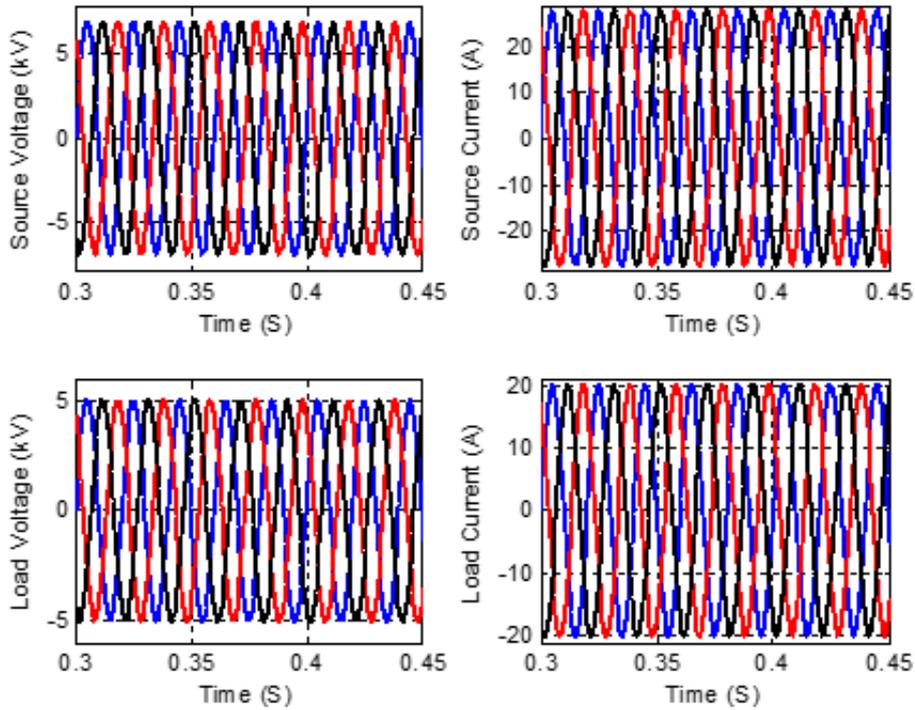


Figure 24: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 6.5 kV and a power of 2 MW

conditions.

As illustrated, the CHB converter is more efficient due to its simpler and fewer components. Typically, the efficiency improves upon increasing voltage and power levels. In turn, the improved overall efficiency indicates that the efficiency
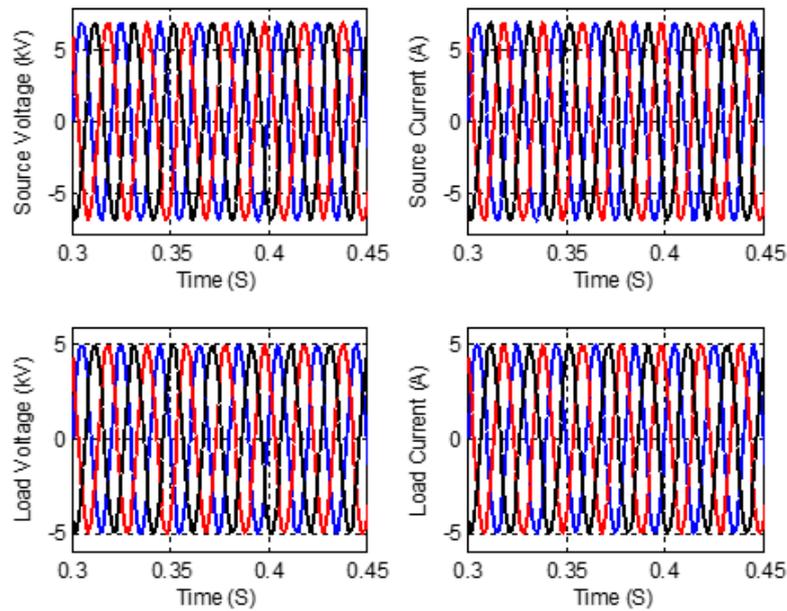
Figure 25: The waveform of voltage and current at the input side and 5L-ANPC load for a voltage of 6.9 kV and a power of 0.5 MW

Table 4: A comparison of the efficiency of converters under various conditions

| Converter's input voltage | 6.9 kV | | 11 kV | | 20 kV | |
|---|---|---|---|---|---|---|
| Power | 0.5 MW | 2 MW | 0.5 MW | 2 MW | 0.5 MW | 2 MW |
| CHB | 89.2 | 90.16 | 90.02 | 90.56 | 90.38 | 90.55 |
| MMC | 86.38 | 88.59 | 87.38 | 88.52 | 86.39 | 88.12 |
| 5L-ANPC | 83.84 | 85.16 | 83.9 | 85.15 | 83.34 | 85.83 |

of the single switches has been enhanced. However, the reason for using more complex converters having a higher number of components is the limitation of power electronic elements in voltage, current, and manufacture.

Table 5 compares the number and capacity of energy storage components in converters under different conditions. The number of energy storage elements in CHB design is less, but the capacity of each part is higher. In other converters, the number of elements is more, and their capacity is less.

Table 5: The DC link capacitance of converters in $\mu F$

| | 6.9 kV | | 11 kV | | 20 kV | |
|---|---|---|---|---|---|---|
| | Inner capacitor | DC link capacitor | Inner capacitor | DC link capacitor | Inner capacitor | DC link capacitor |
| CHB | Six 1250 capacitors | Six 2500 capacitors | Six 1250 capacitors | Six 2500 capacitors | Six 1250 capacitors | Six 2500 capacitors |
| MMC | A 370 capacitor in each module, four 250 capacitors in each module | 2000 | A 370 capacitor in each module, four 250 capacitors in each module | 2000 | A 370 capacitor in each module, four 250 capacitors in each module | 2000 |
| 5L-ANPC | Two 670 capacitors | 2000 | Two 670 capacitors | 2000 | Two 670 capacitors | 2000 |

Table 6 compares the number of parts in the converters. When the converter is more straightforward, the number of components decreases, and the voltage and current level in the parts rise at the same power and voltage. It is also true for voltage and current levels in IGBTs.

Table 6: The number of parts in converters

| Converter | Number of parts |
|-----------|-----------------|
| CHB       | 19              |
| MMC       | 56              |
| 5L-ANPC   | 47              |

## 7 Conclusion

In this paper, a three-phase solid-state transformer (SST) based on multi-level converters, including CHB, MMC, and Cascaded ANPC, has been efficiently designed and controlled for three voltage levels, and the operational parameters of the SST have been investigated and compared for two power levels. The results of this paper are summarized as follows:

- The CHB converter is more efficient due to its simpler and fewer parts.

- Generally, the efficiency improves upon increasing voltage and power levels.

- The number of energy storage elements in the CHB design is less, but the capacity of each element is higher. In other converters, the number of elements is more, and their capacity is less.

- When the converter is more straightforward, the number of parts decreases, and the voltage and current levels in the parts increase at the same power and voltage. It is also true about voltage and current levels in IGBTs.

- To get a better control effect on the MCs system, hierarchical control strategies were used.

The utilized voltage stress and switch currents in the under-study SSTs vary in different power and voltage levels, and they have been referred to in the Tables of this paper. Therefore, at different levels of voltage and power, due to efficiency, loss and volume, the best structure can be selected.

## References

[1] F.B. Ajaei and R. Iravani, *Dynamic interactions of the MMC-HVDC grid and its Host AC system due to AC-Side disturbances*, IEEE Trans. Power Delivery **31** (2016), no. 3, 1289–1298.

[2] B.K. Bose, *Power electronics and motor drives recent progress and perspective*, IEEE Trans. Ind. Electron. **56** (2009), no. 2, 581–588.

[3] Dasgupta, *Design of Transformers*, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2002.

[4] L. Ferreira Costa, G.D. Carne, G. Buticchi and M. Liserre, *The Smart Transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid*, IEEE Power Electron. Magazine. **4** (20017), no. 2, 56–67.

[5] L.G. Franquelo, J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo and M.A.M. Prats, *The age of multilevel converters arrives*, IEEE Ind. Electron. Mag. **2** (2008), no. 2, 28–39.

[6] F. Haase, A. Kouchaki and M. Nymand, *Controller design and implementation of a three-phase Active Front End using SiC based MOSFETs*, 9th Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia), 2015, pp. 2681–2687.

[7] S. Kakar, Sh. Bin Md. Ayob, A. Iqbal, N. Mohamad Nordin, M. Saad Bin Arif and Sh. Gore, *New asymmetrical modular multilevel inverter topology with reduced number of switches*, IEEE Access **9** (2021) 27627–27637.

[8] J. Rodriguez, B. Wu, S. Bernet, N. Zargari, J. Rebolledo, J. Pontt and P. Steimer, *Design and evaluation criteria for high power drives*, Conf. Rec. IEEE IAS Annu. Meeting, 2008, pp. 1–9.

[9] F. Rojas, M. Díaz, M. Espinoza and R. Cárdenas, *A solid state transformer based on a three-phase to single-phase Modular Multilevel Converter for power distribution networks*, Power Electron. Conf. (SPEC), 2017, pp. 1.

[10] J. Rodriguez, L.G. Franquelo, S. Kouro, J.I. Leon, R.C. Portillo, M.A.M. Prats and M.A. Perez, *Multilevel converters: An enabling technology for high-power applications*, Proc. IEEE. **97** (2009), no. 11, 1786–1817.

[11] A. Marzoughi, R. Burgos, D. Boroyevich and Y. Xue, *Design and Comparison of Cascaded H-bridge, Modular Multilevel Converter and 5-L Active Neutral Point Clamped Topologies for Motor Drive Applications*, IEEE Trans. Ind. Appl. **54** (2018), no. 2, 1404–1413.

[12] G. Mondal and S. Nielebock, *Control of M2C direct converter for AC to AC conversion with wide frequency range*, 18th Eur. Conf. Power Electron. Appl. (EPE'16 ECCE Europe), 2016, pp. 1–10.

[13] M.M. Swamy, J.K. Kang and K. Shirabe, *Power loss, system efficiency, and leakage current comparison between Si IGBT VFD and SiC FET VFD with various filtering options*, IEEE Trans. Ind. Appl. **51** (2015), no. 5, 3858–3866.